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MS-7A12

Intel -Skylake plamform Z170

ATX

Ver: 1.1

CPU:

Skylake-S

System Chipset:

Z170

Onboard Chip:

HD Audio Codec:ALC1150

LAN:Intel I219V

SIO:Nuvoton 6793D

Flash ROM: SPI 128MB

Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI:

NIKO/UPI

PWM:

IMVP8 -ISL95856

Expansion Slots:

PCI Express (X16) Slot *1

PCI Express (X8) Slot * 1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 4

M2 * 1

SATAe* 1

SATA3.0 x4

Other:

REAR USB2.0 *4

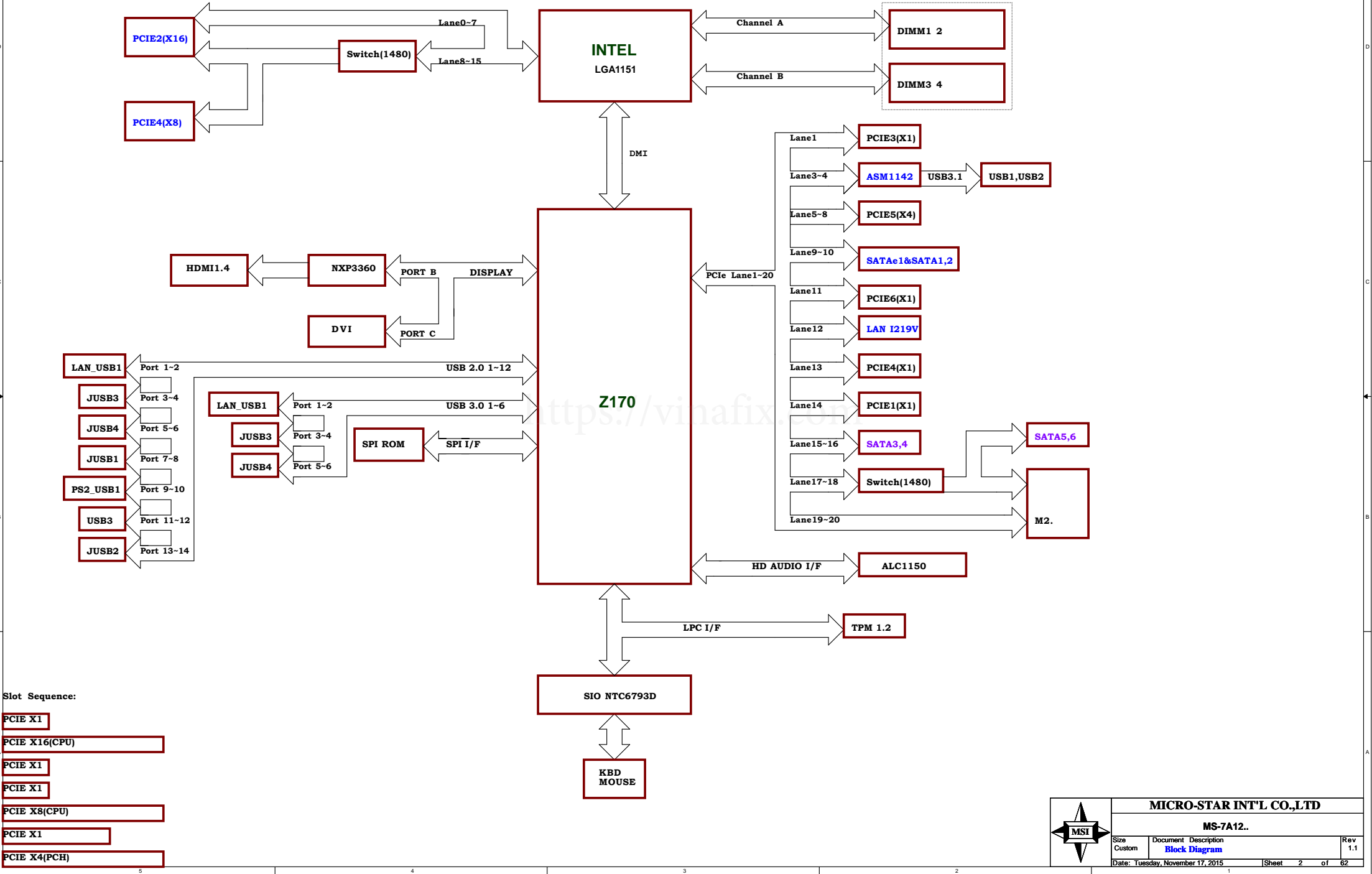
REAR USB3.0 *2

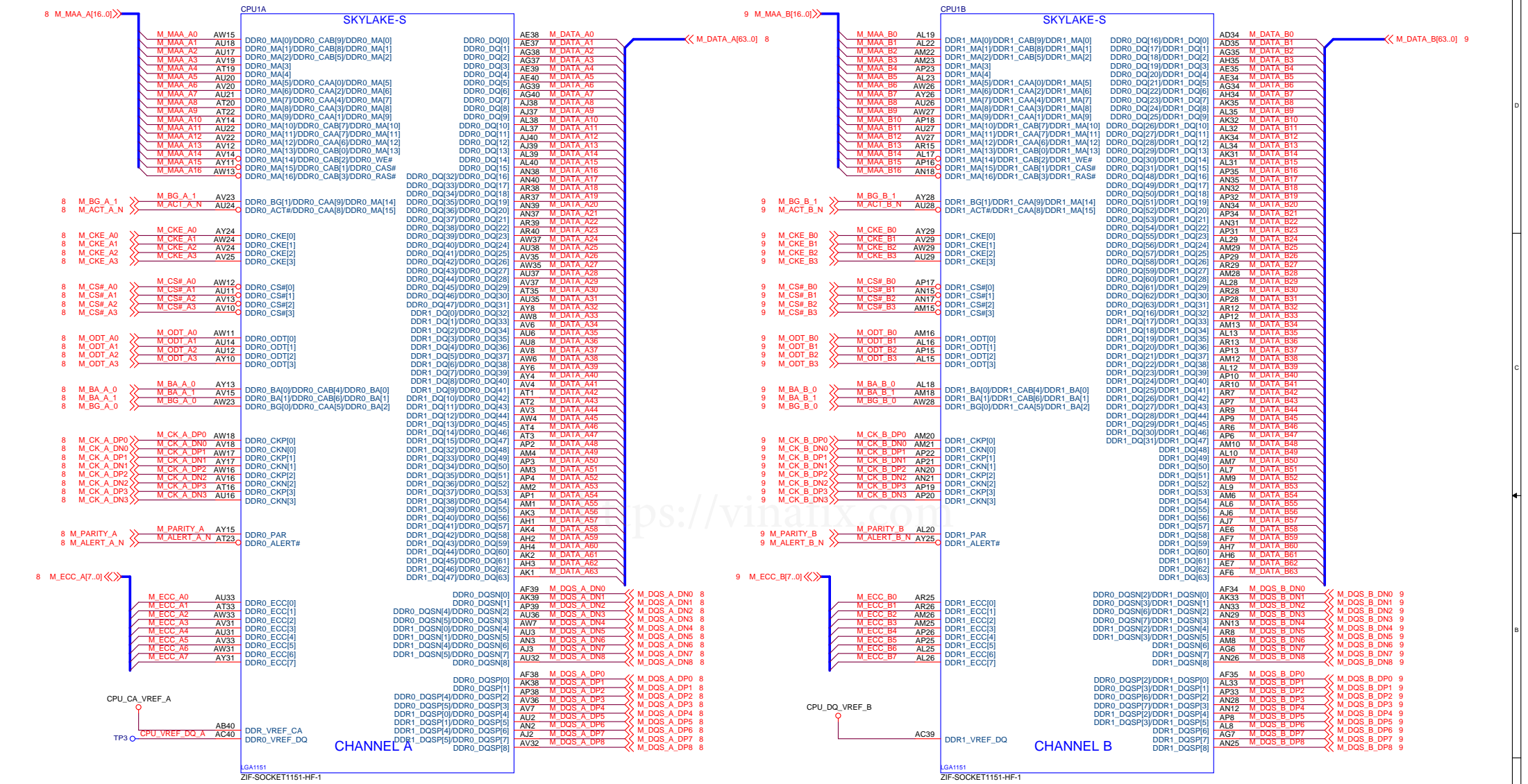
REAR USB3.1 *2

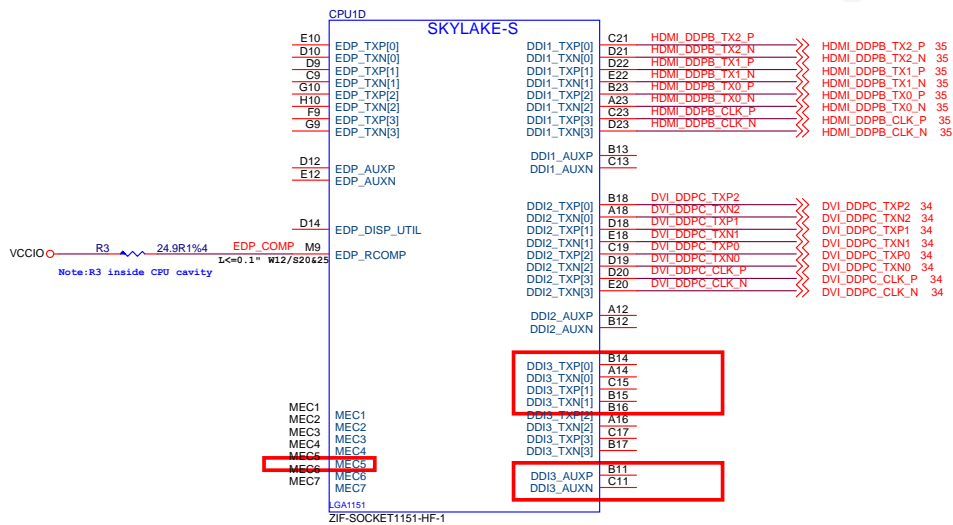
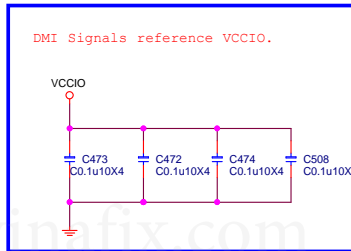
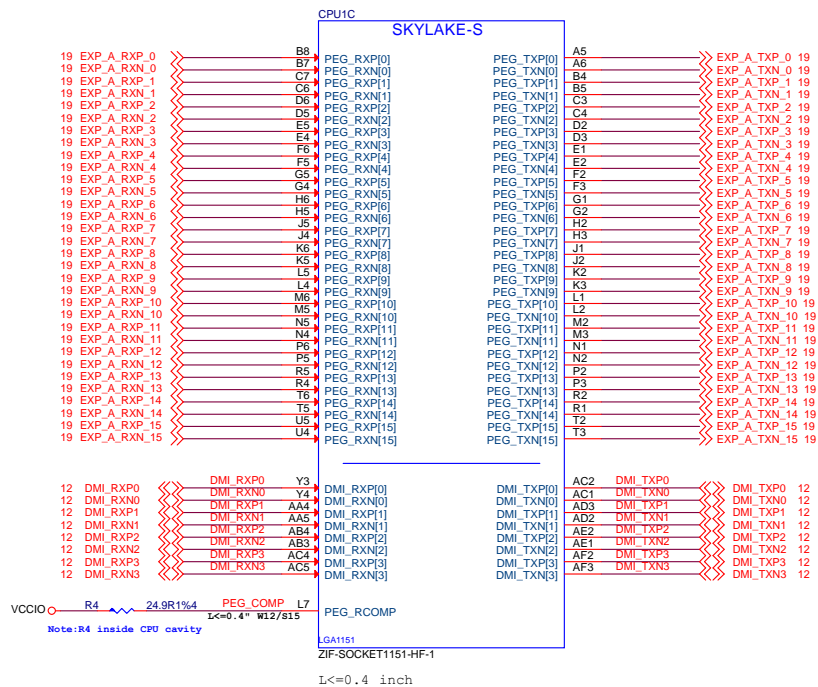
FRONT USB2.0 *4

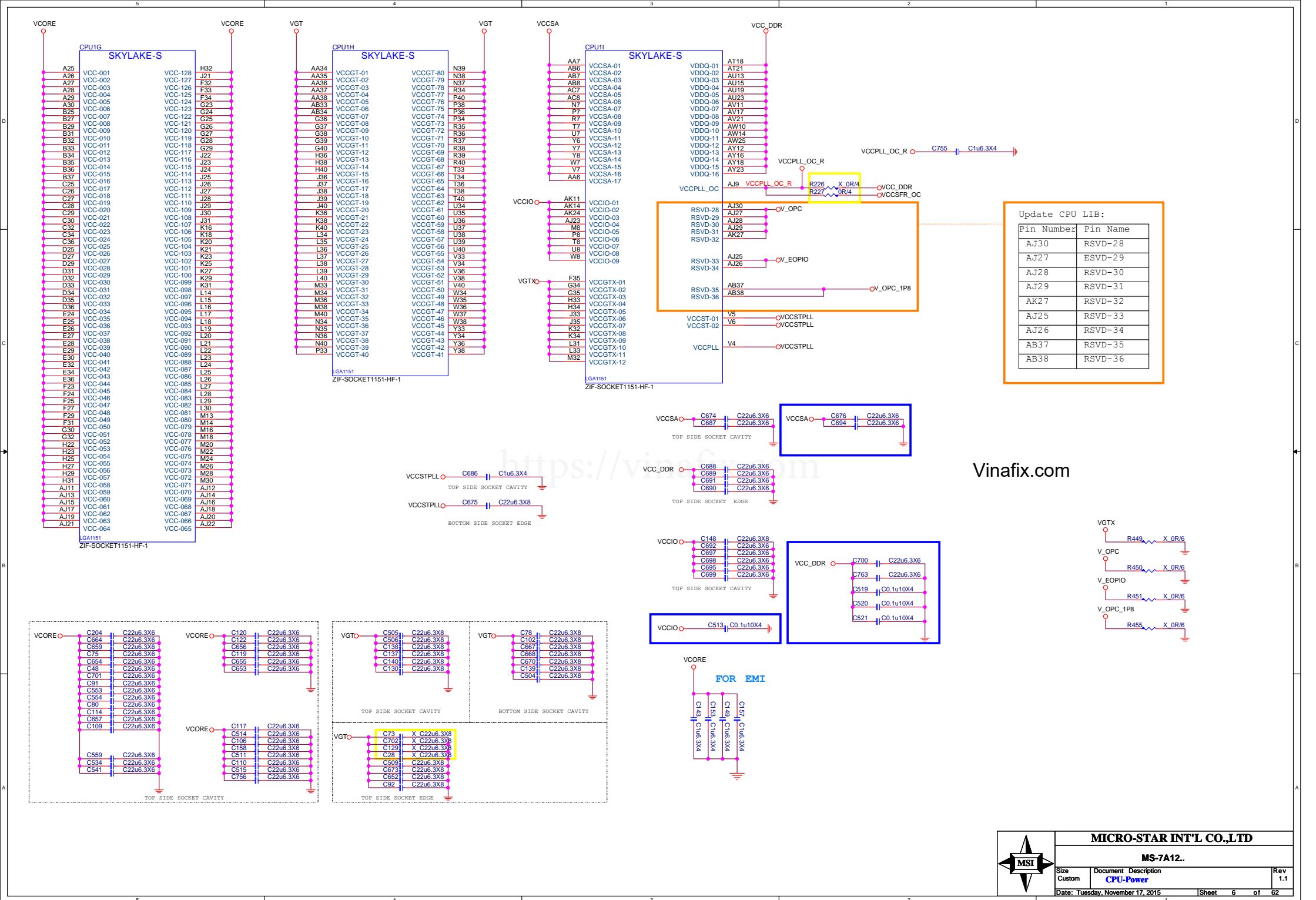
FRONTUSB3.0 *4

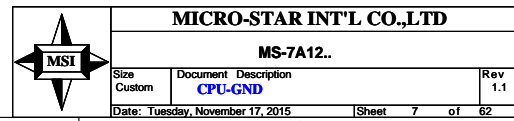
MS-7A12 Block Diagram

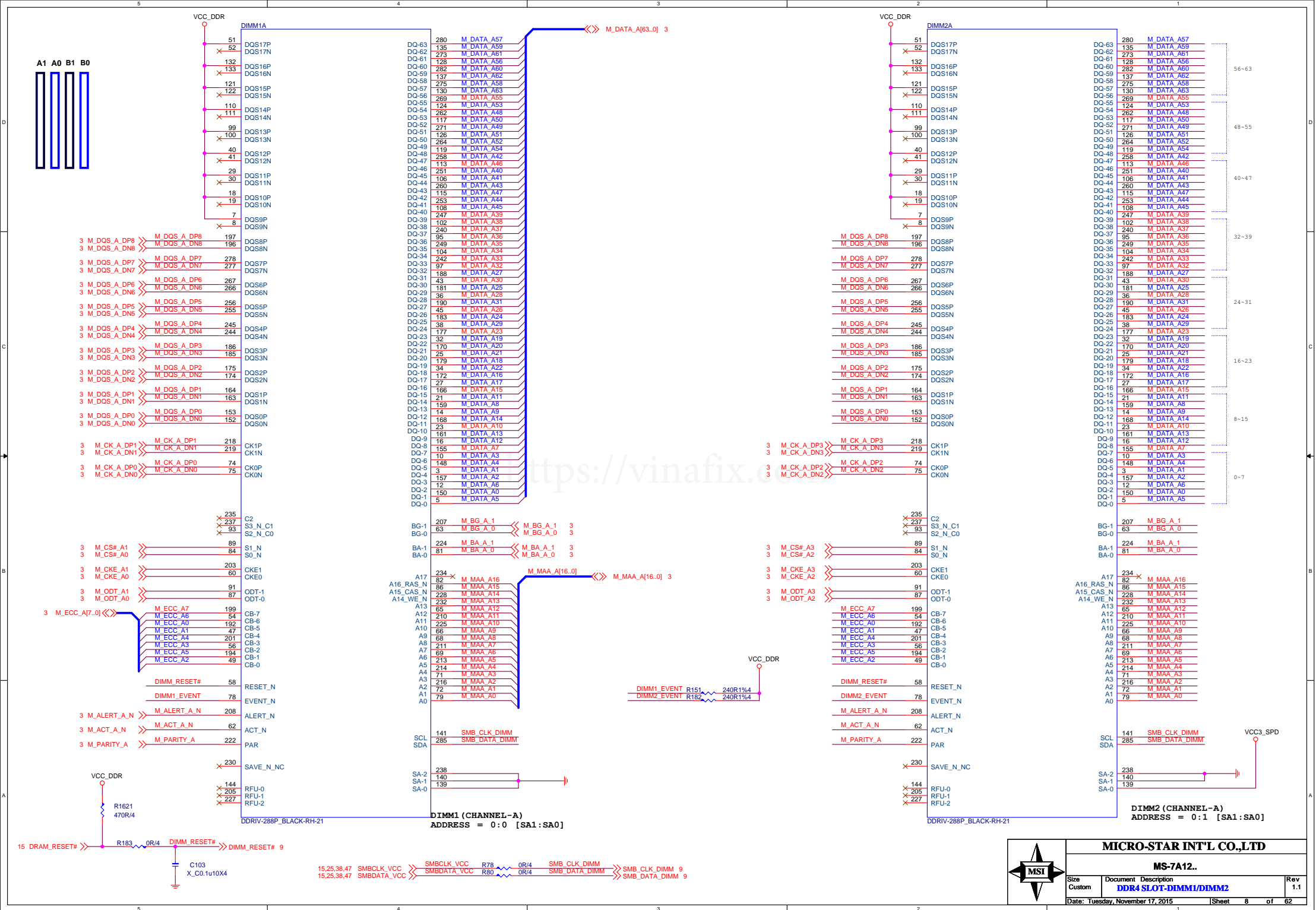


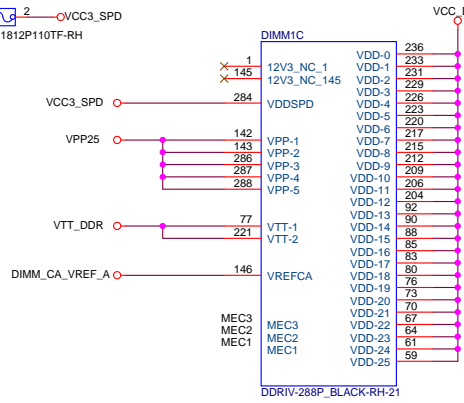
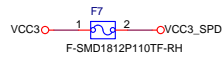




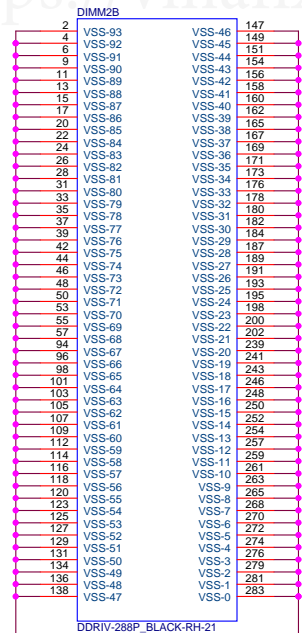
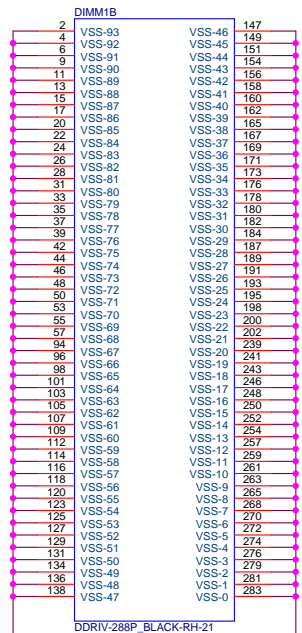
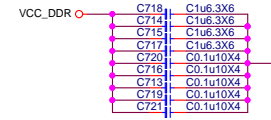
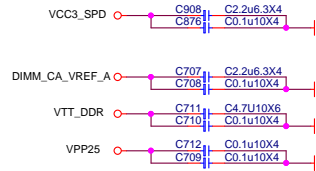
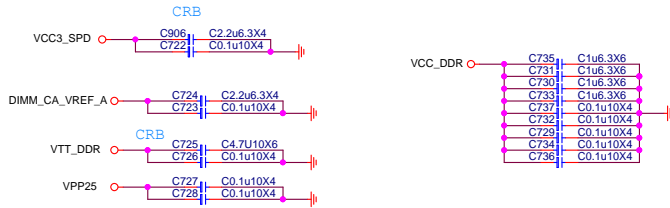
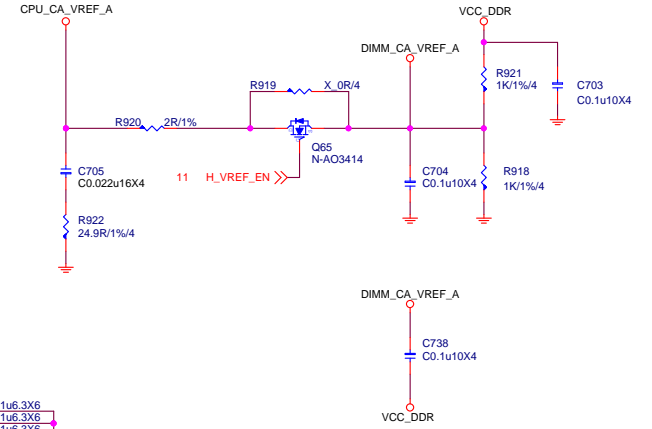
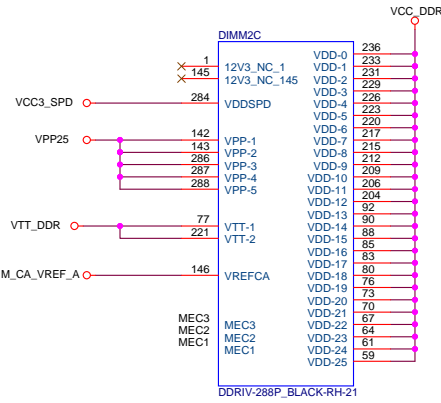
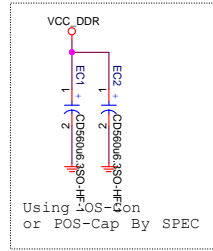


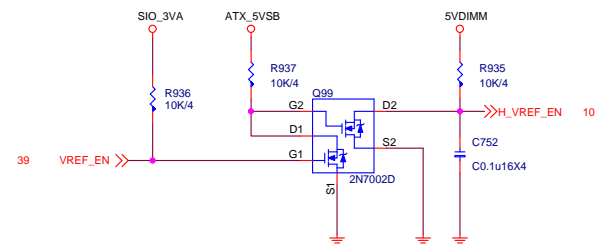
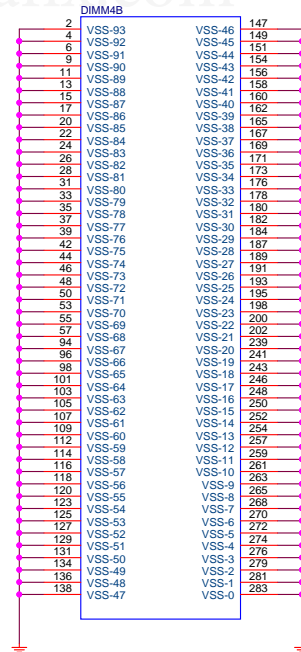
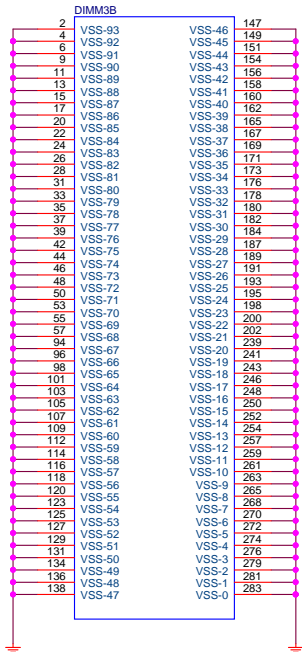
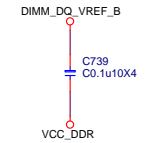
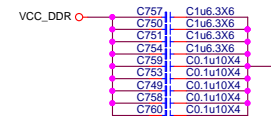
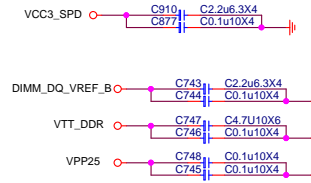
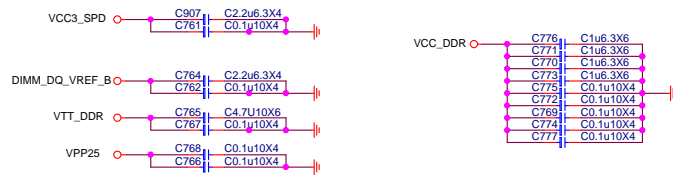
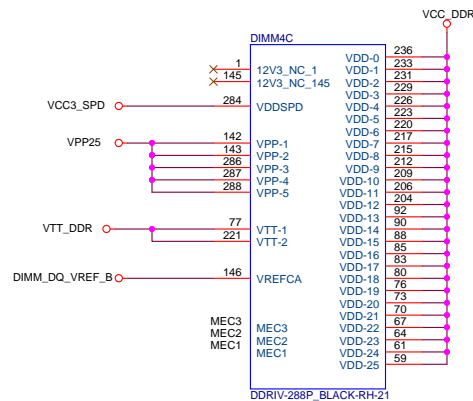






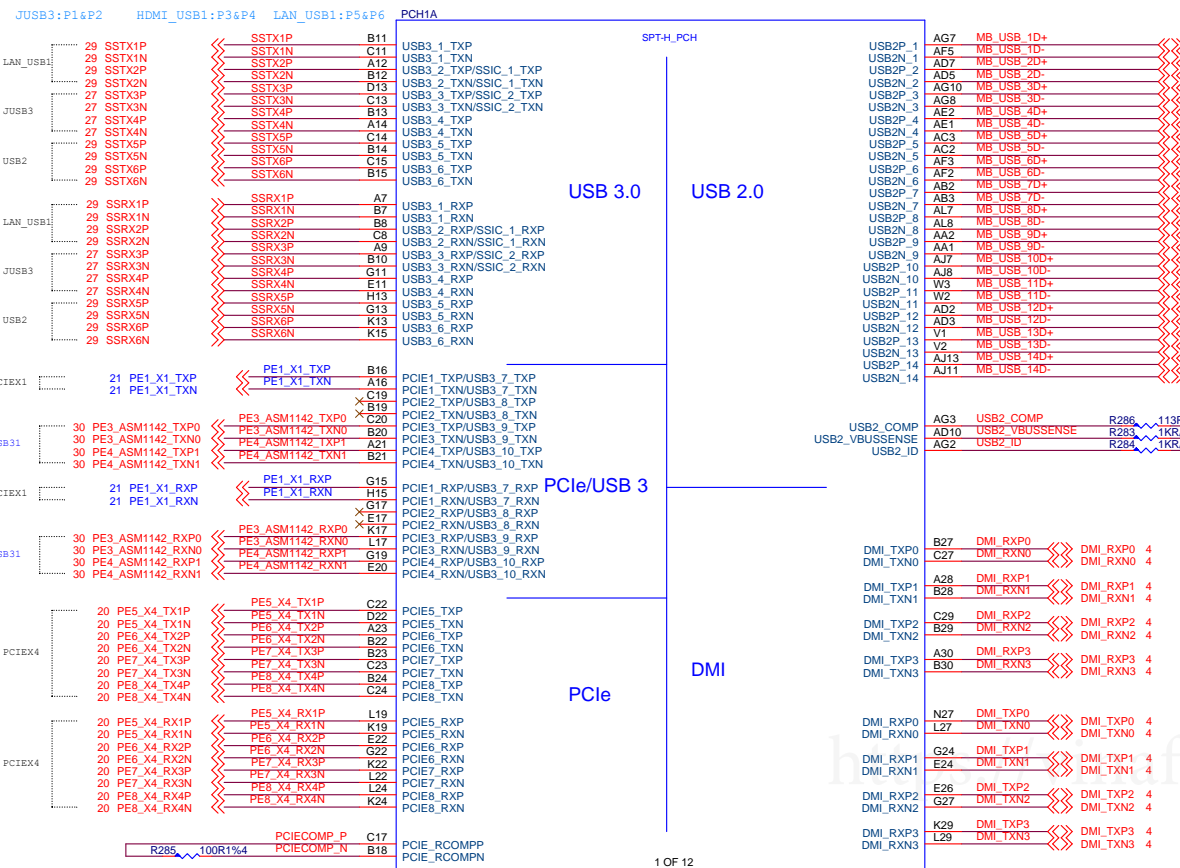
DIMM SLOT PN BY SPEC





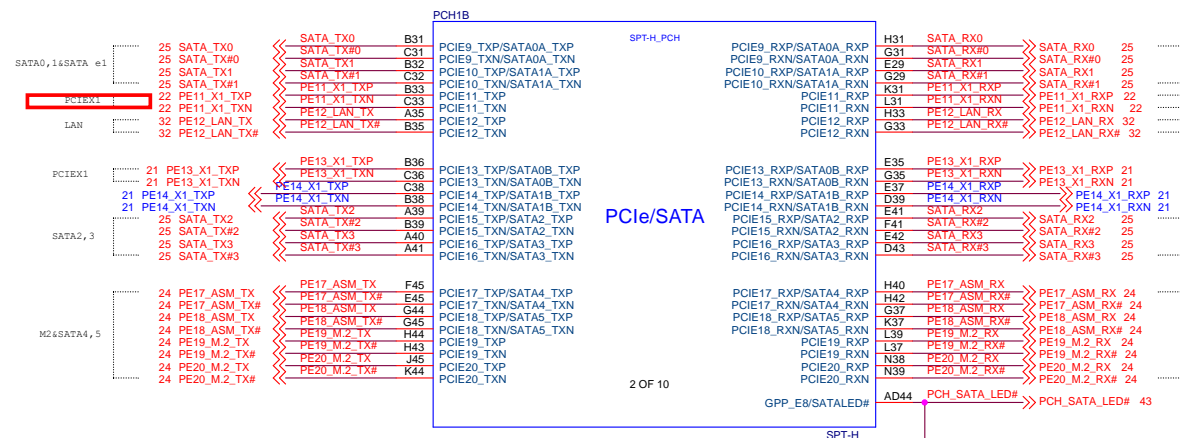
MS-7A12..


Size Custom	Document Description DDR4-POWER/GND-2	Rev 1.1
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sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCie/ LAN	PCie	PCie	PCie
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCie/ LAN	PCie	PCie	PCie
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCie	PCie/ LAN	PCie/ LAN	PCie	PCie	PCie
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCie	USB3/ PCie	USB3/ PCie	USB3/ PCie/ LAN	PCie/ LAN	PCie	PCie	PCie

Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCie/ LAN	PCie	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCie/LAN	PCie/ SATA*	PCie	PCie/ LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	N/A	0
H170	PCie/LAN	SATA	PCie	PCie/ LAN	SATA	SATA	SATA	SATA	SATA	PCie	PCie	PCie	2
Z170	PCie/LAN	PCie/ SATA	PCie	PCie/ LAN	SATA	SATA	SATA	SATA	SATA	PCie	PCie	PCie	3



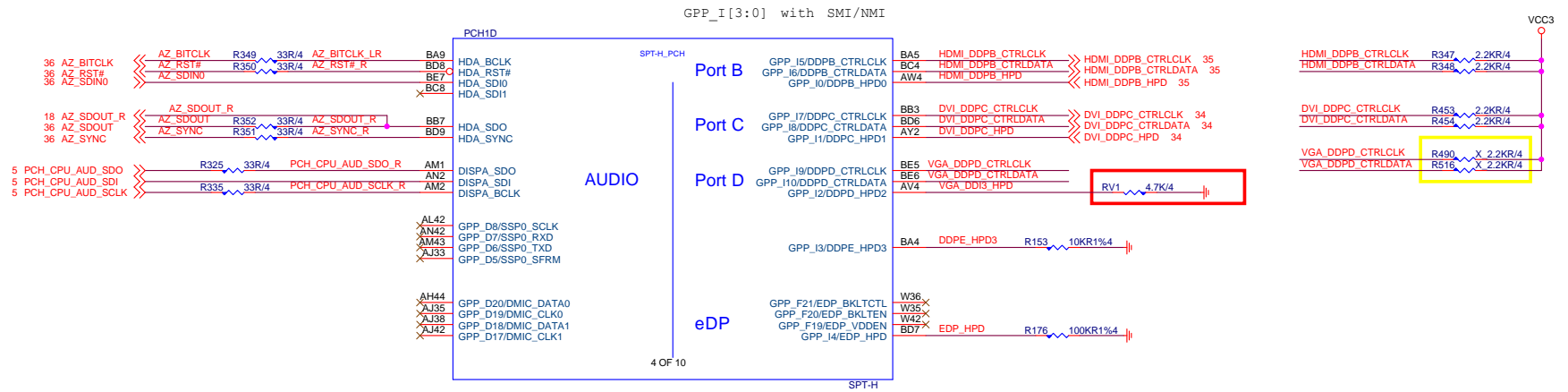


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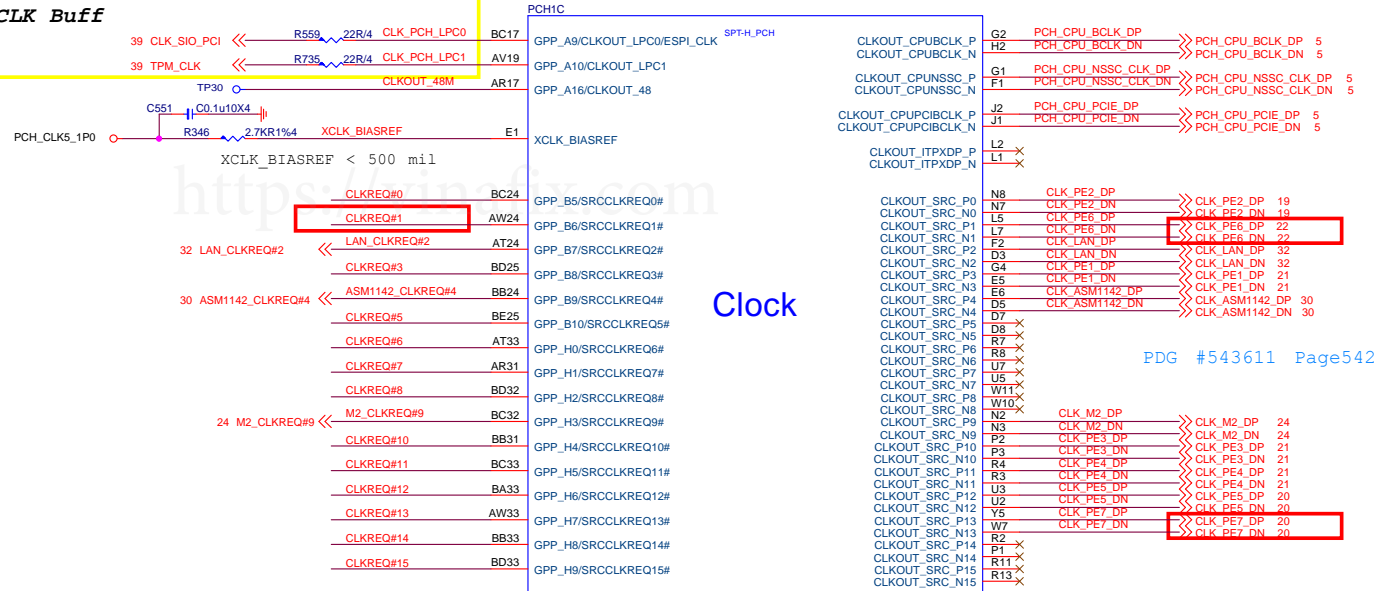
MS-7A12..

Size Custom Document Description Rev 1.1

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Remove CLK Buff



Clock

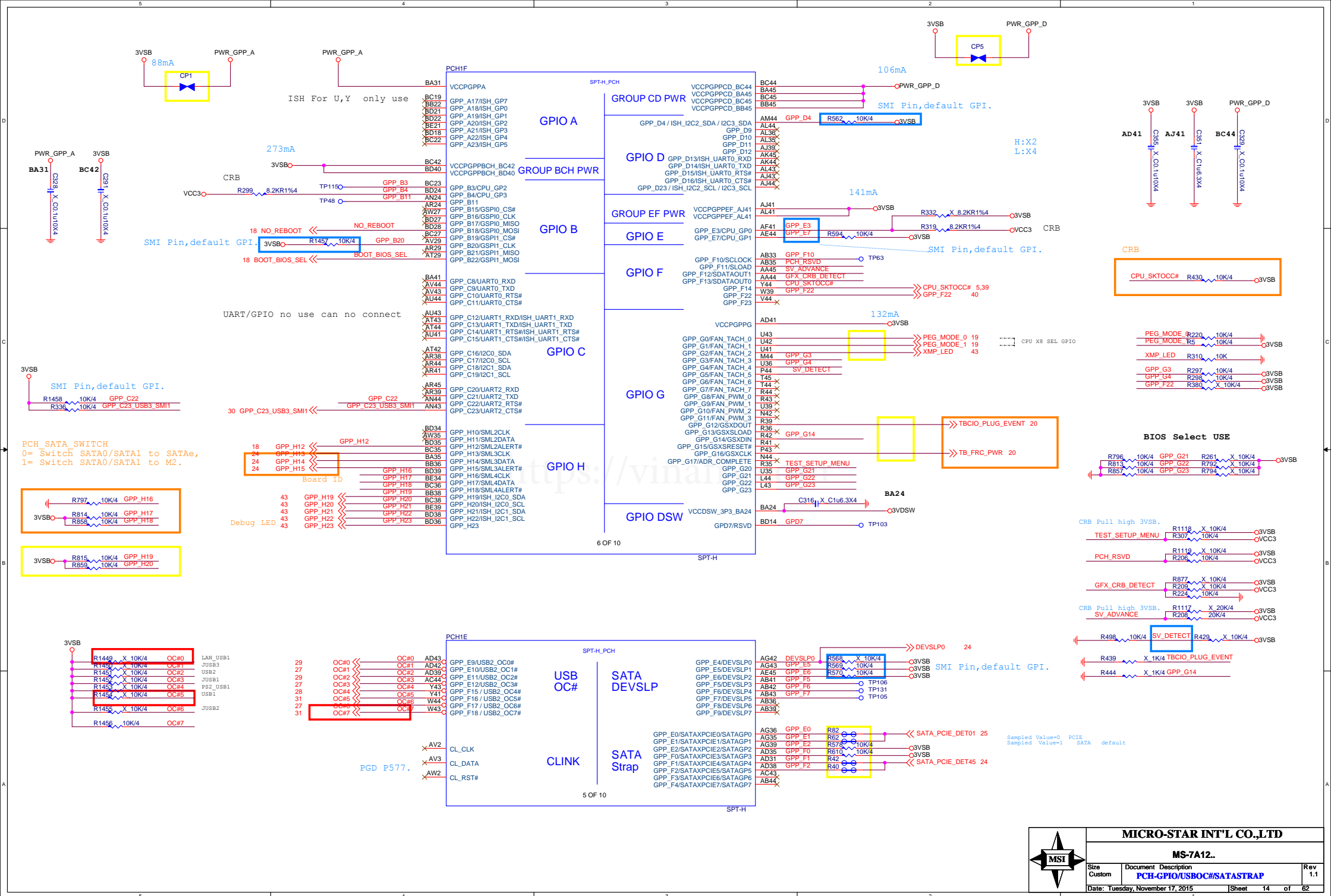
PDG #543611 Page542



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MS-7A12..

Size	Document	Description	Rev
Custom		PCH-Audio/Display/Clock	1.1
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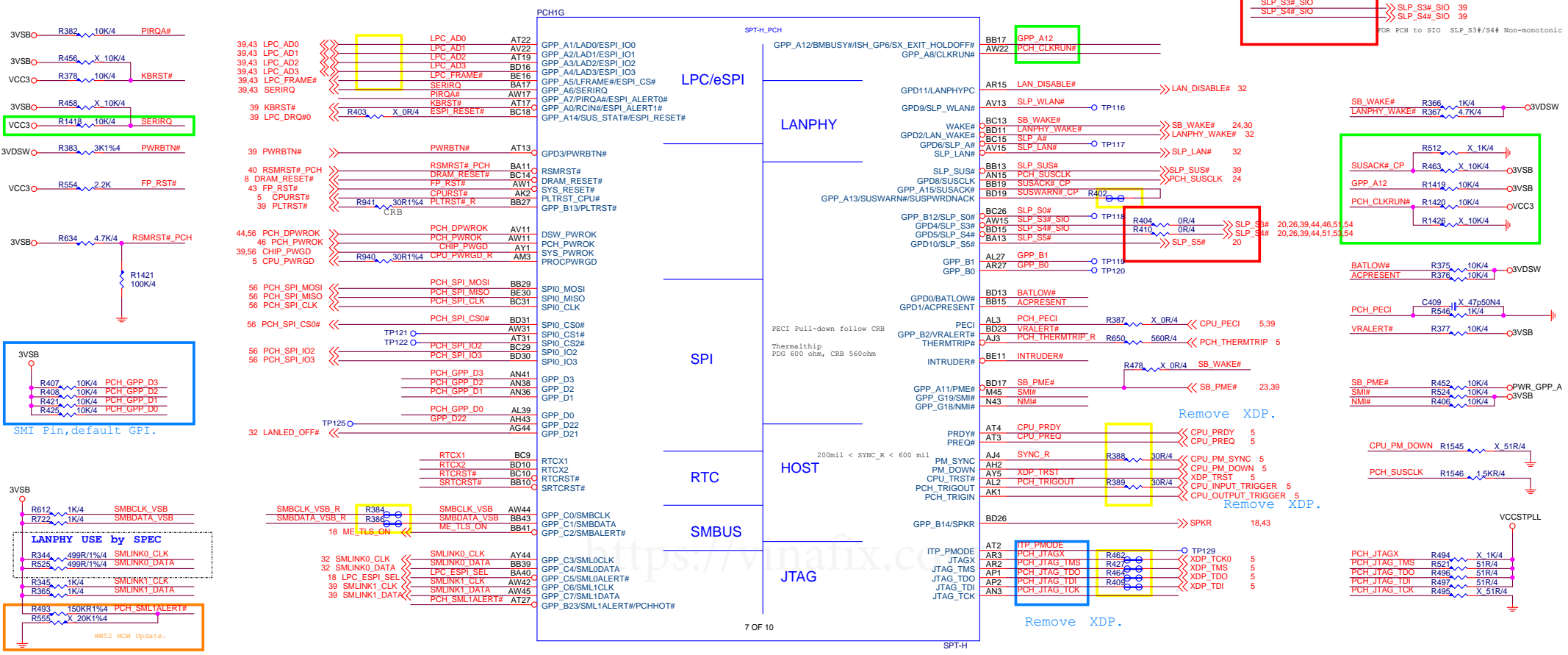
MICRO-STAR INT'L CO.,LTD

MS-7A12..

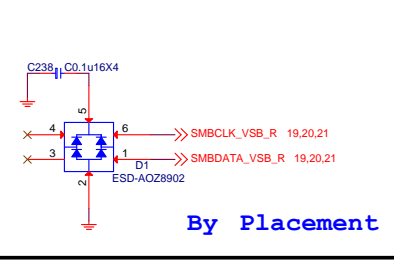
Size Custom	Document Description PCH-GPIO/USBOC#/SATASTRAP
----------------	--

Rev
1.1

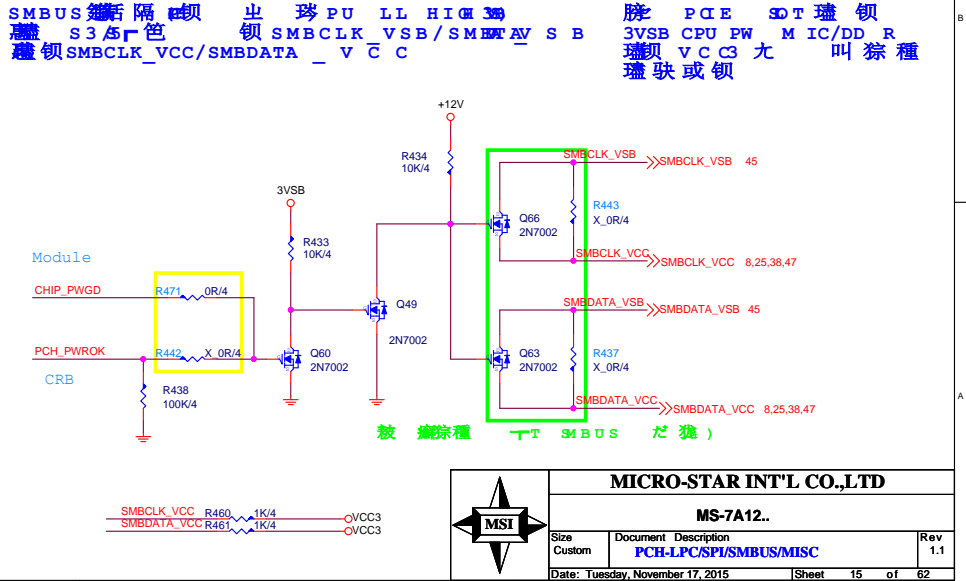
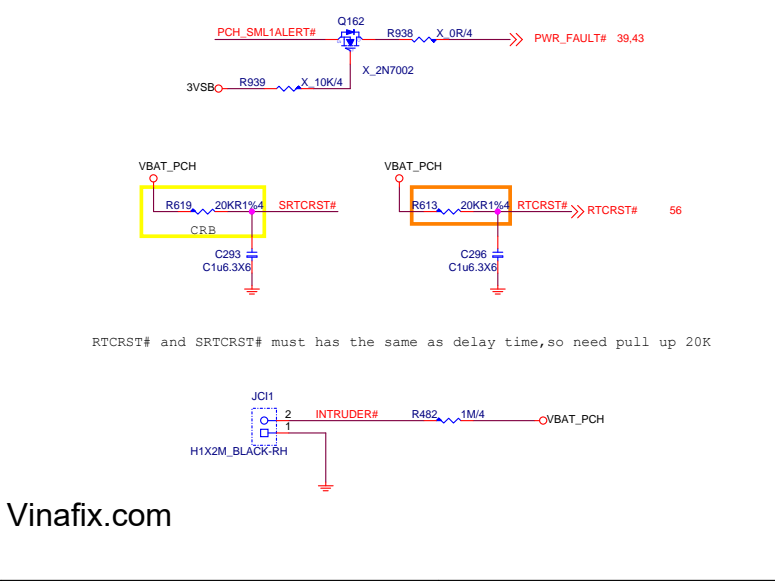
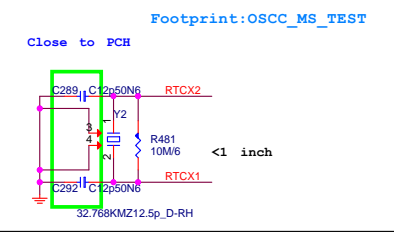
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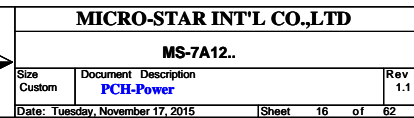
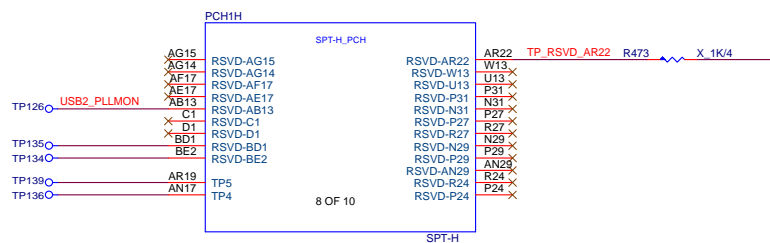
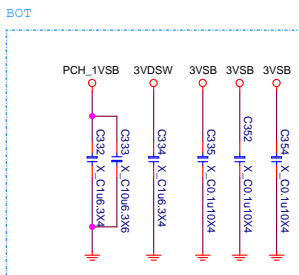
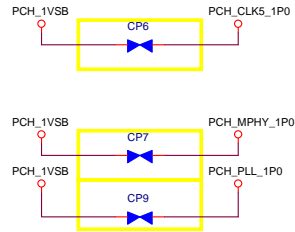


SMBUS ESD



RTC Block

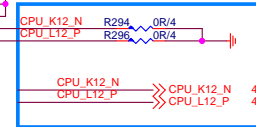




GND

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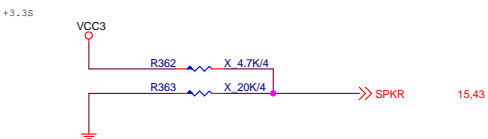


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MS-7A12..

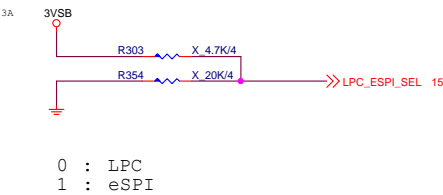
Size	Document	Description	Rev
Custom		PCH-GND	1.1
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TOP Swap



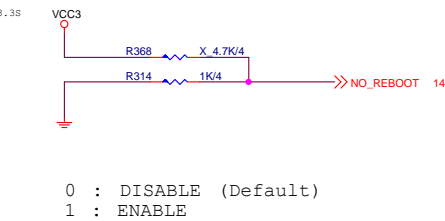
Internal pull-down is disabled after PLTRST#

LPC eSPI Mode



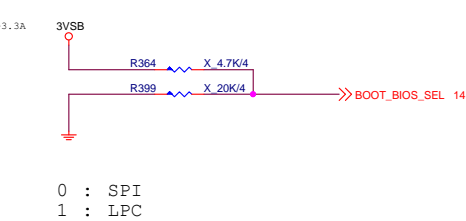
Internal pull-down is disabled after RSMRST

No Reboot



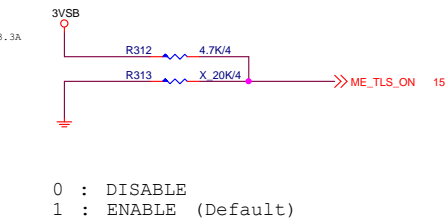
Internal pull-down is disabled after PLTRST#

Boot BIOS



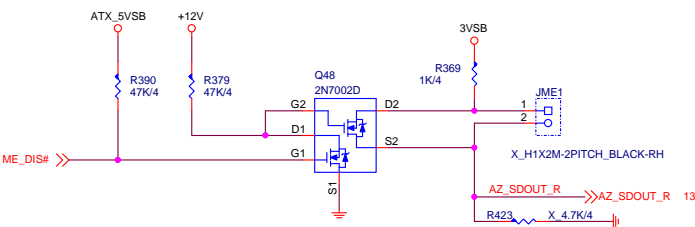
Internal pull-down is disabled after PLTRST

AMT and SBA with confidentiality

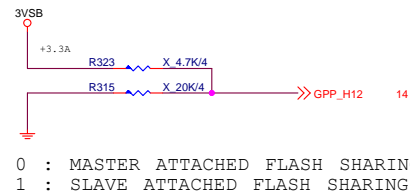


Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE

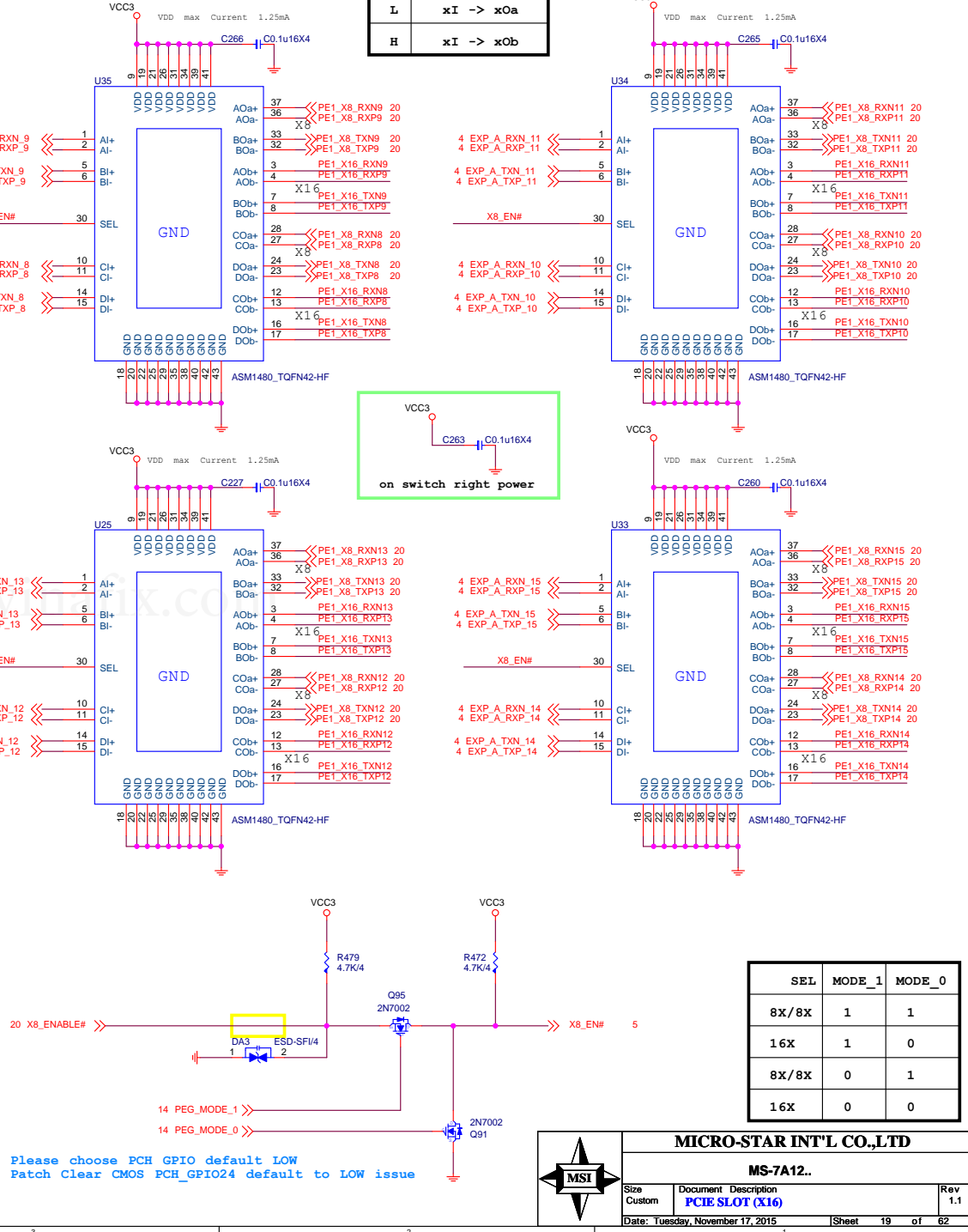


Internal pull-down is disabled after RSMRST



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MS-7A12..		
Size	Document	Description
Custom		PCH-Strap
Date: Tuesday, November 17, 2015	Sheet 18 of 62	Rev 1.1

```
support max_speed GEN3 Black
```

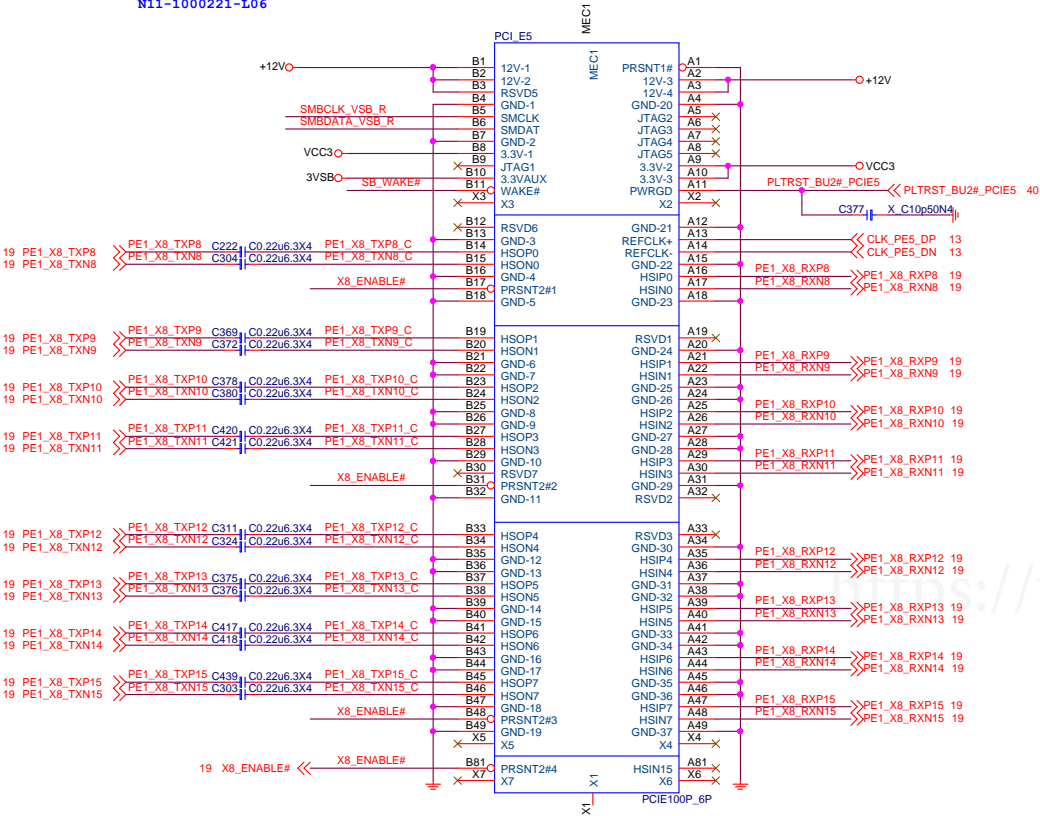


PCI Express X8 Slot

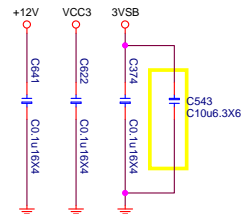
support max speed GEN3

Black

footprint: ON1-7968001
N11-1000221-L06



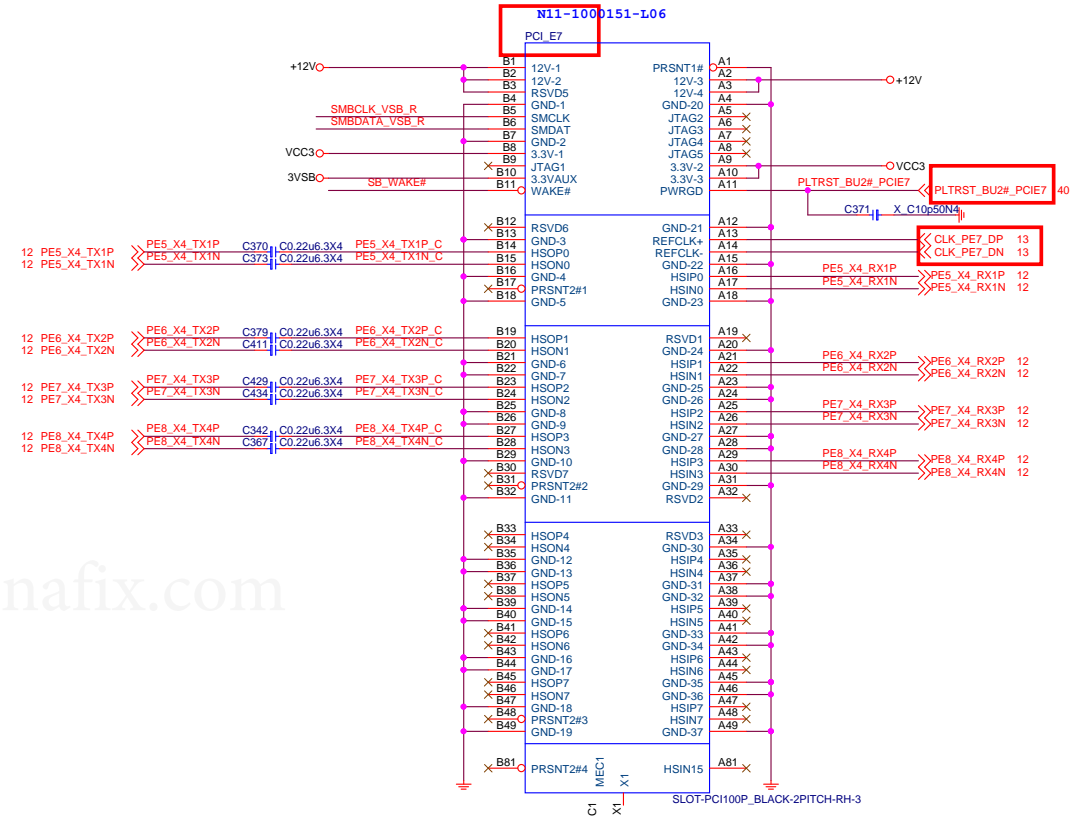
EMI:close pin



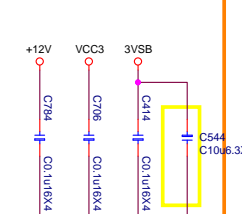
PCI Express X4 Slot

support max speed GEN3

Black

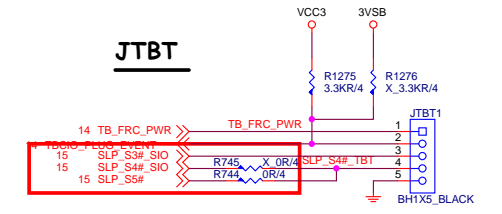


EMI:close pin



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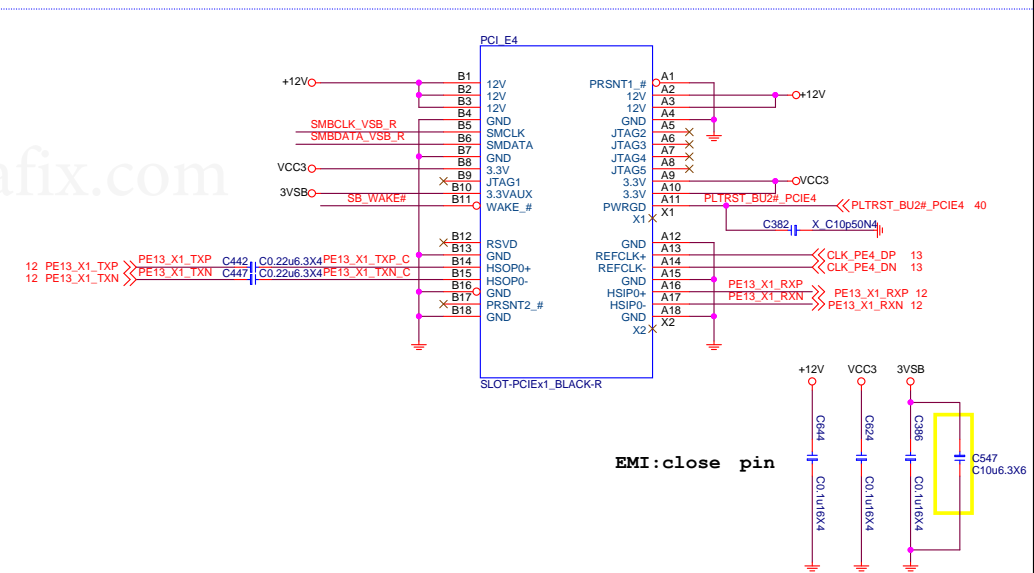
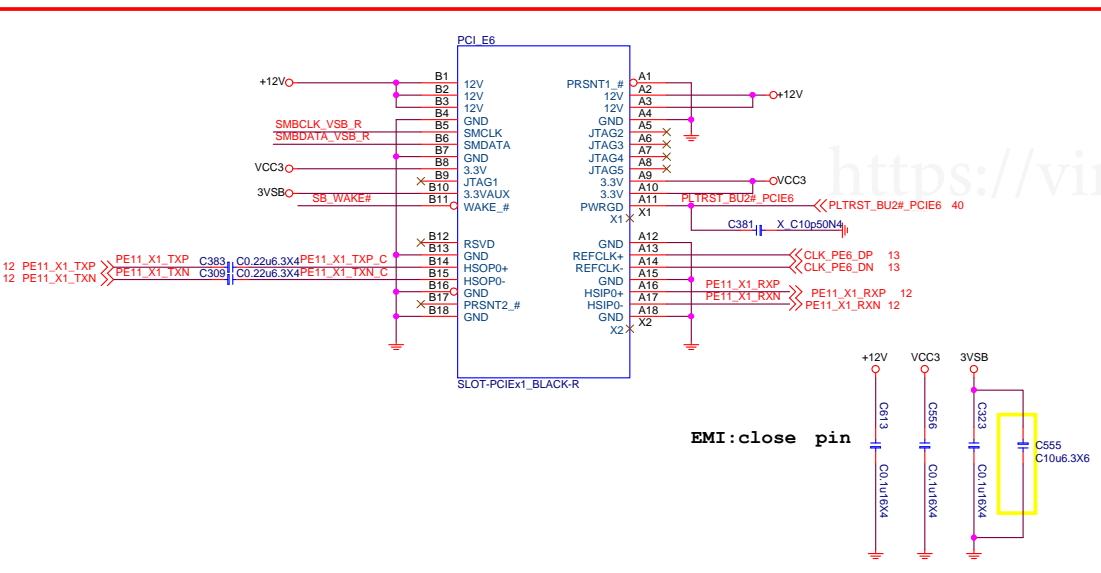
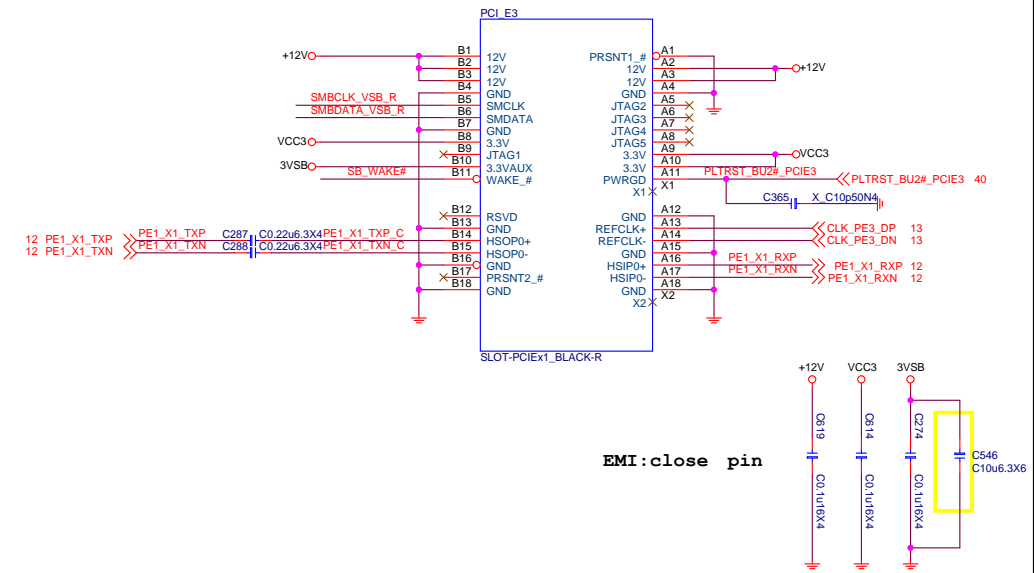
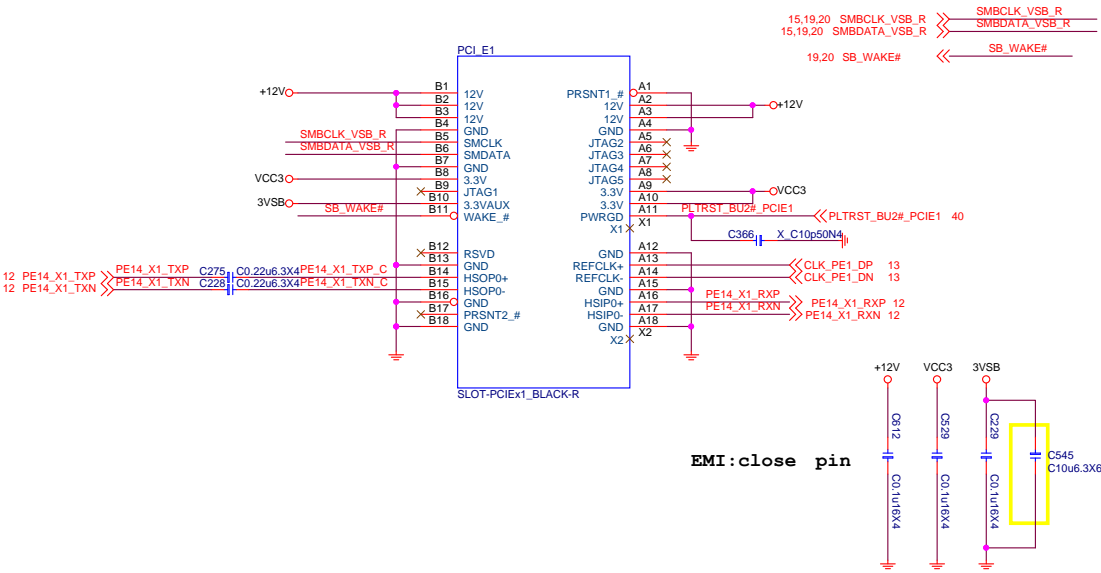
JTBT



MICRO-STAR INT'L CO.,LTD

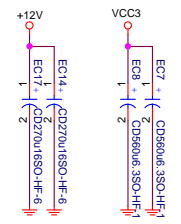
MS-7A12..

Size	Document	Description	Rev
Custom		PCIE SLOT (X4)	1.1
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PCIE (X1) *4 PCIE (X4) *1 PCIE (X8) *1 PCIE (X16) *1

3.3Vaux: 0.375*7=2.625A (wake)
0.02*5=0.14A (no wake)
VCC3: 3*7=21A
+12V: 0.5*4+2.1+2.1+5.5=11.7A




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Size	Document	Description	Rev
Custom		PCIE SLOT (X1)	1.1

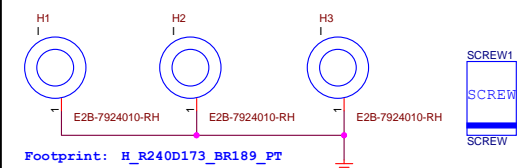
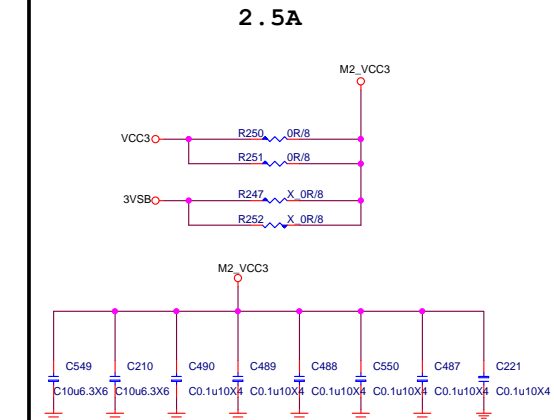
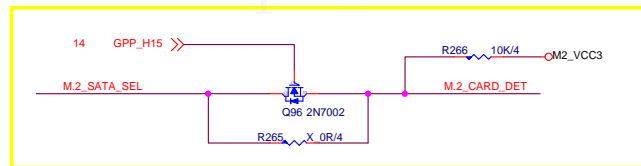
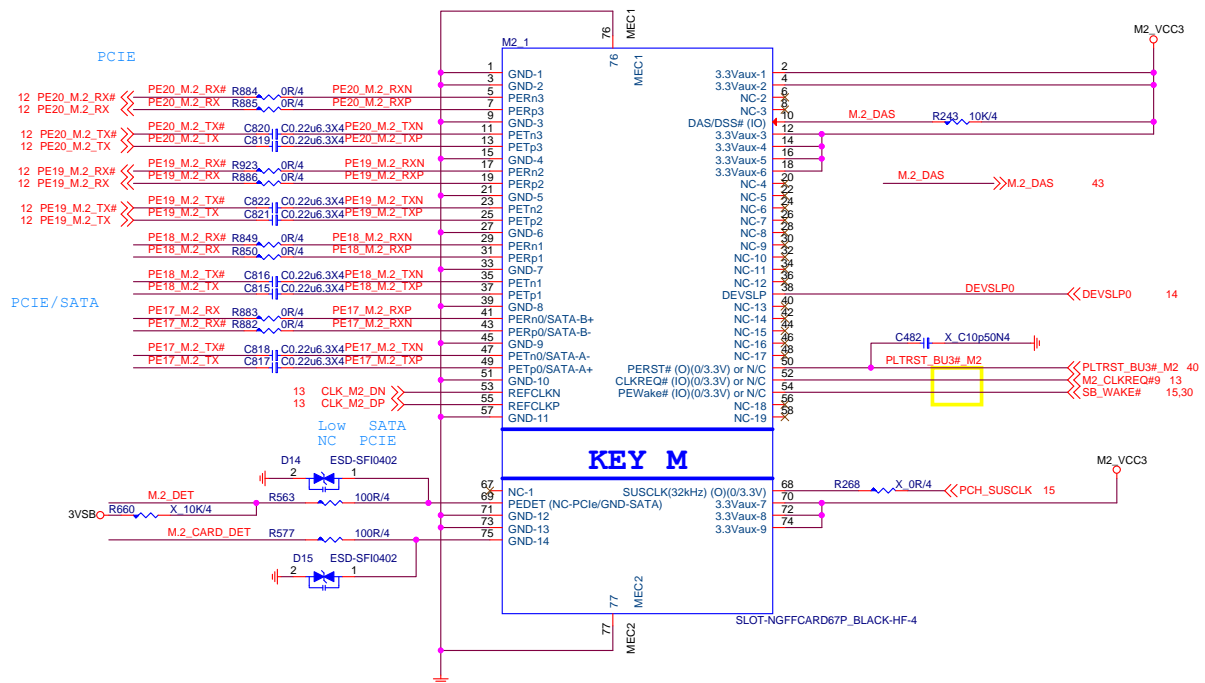
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	MS-7A12..		
Size Custom	Document PCIE to PCI-ASM1083	Description	Rev 1.1
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	MICRO-STAR INT'L CO.,LTD	
	MS-7A12..	
Size Custom	Document Description PCI SLOT	Rev 1.1
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	SATA CARD	PCIE CARD	NA	NO CARD
SATA_PE_DET	0	1	0	1
M.2_CARD_DET	0	0	1	1
SATA4/5GP				
1 SATA MODE 0 PCIE MODE	1	0	1	1

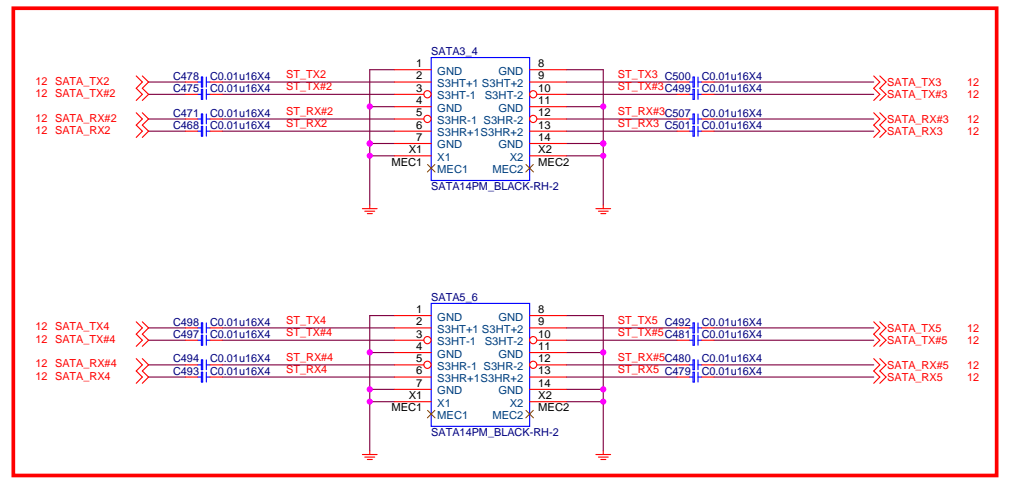
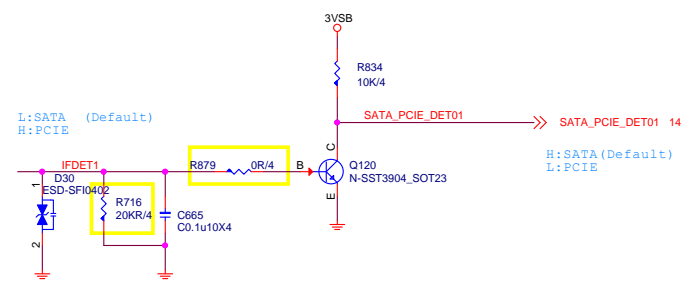
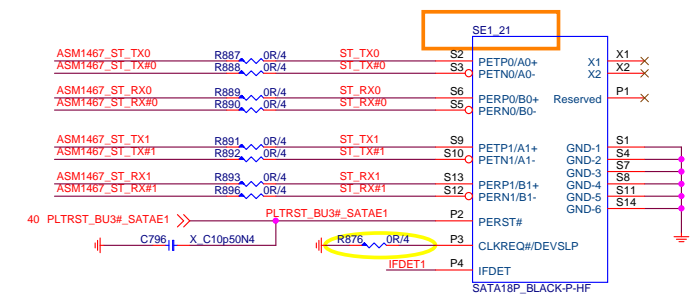
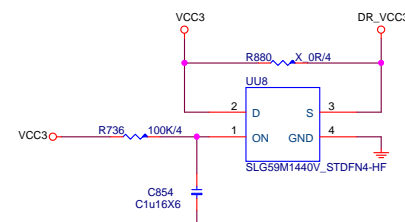
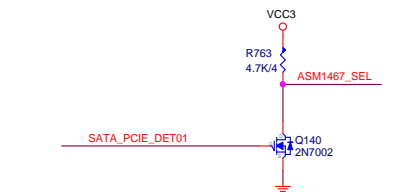
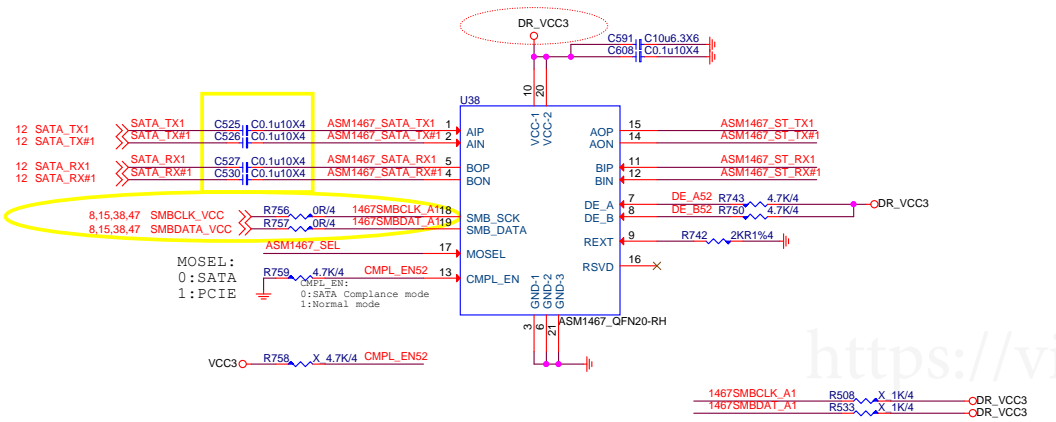
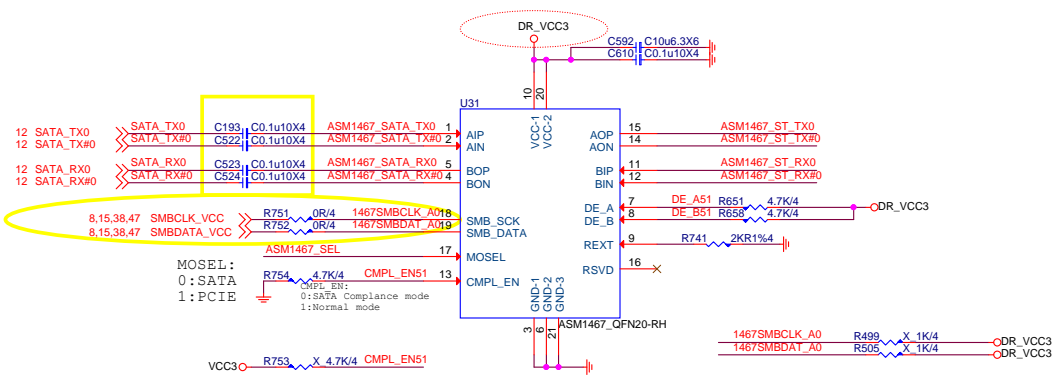
SATA4GP/SATA5GP
for chipset that main power, if pull up to VSB maybe will leakage power
If sampled value = 1, select SATA; if sampled value = 0, select PCIE



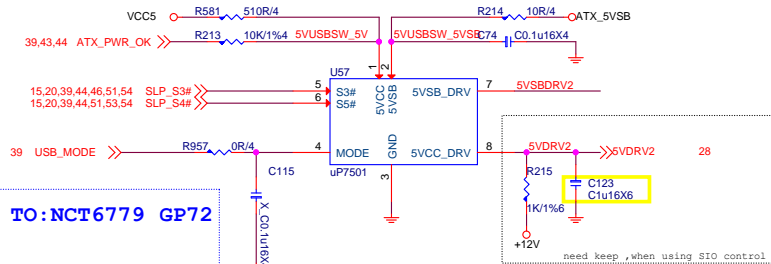
MICRO-STAR INT'L CO.,LTD

MS-7A12..

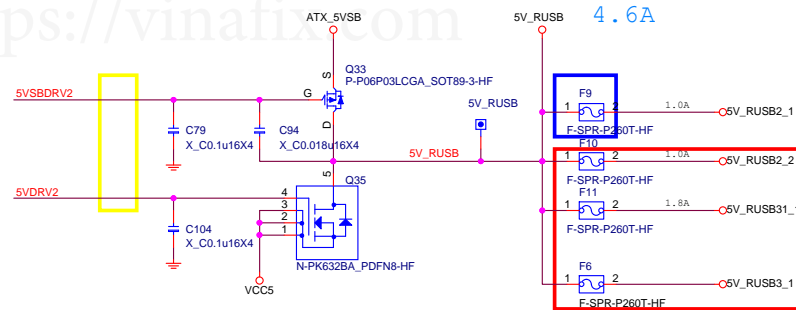
Size Custom	Document Description M.2 Card SLOT	Rev 1.1
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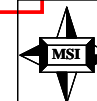
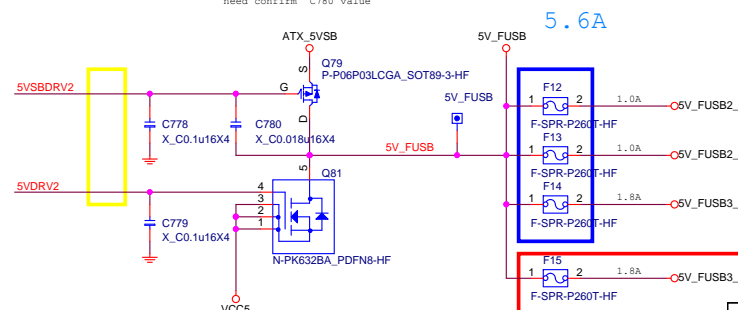
5VSBDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

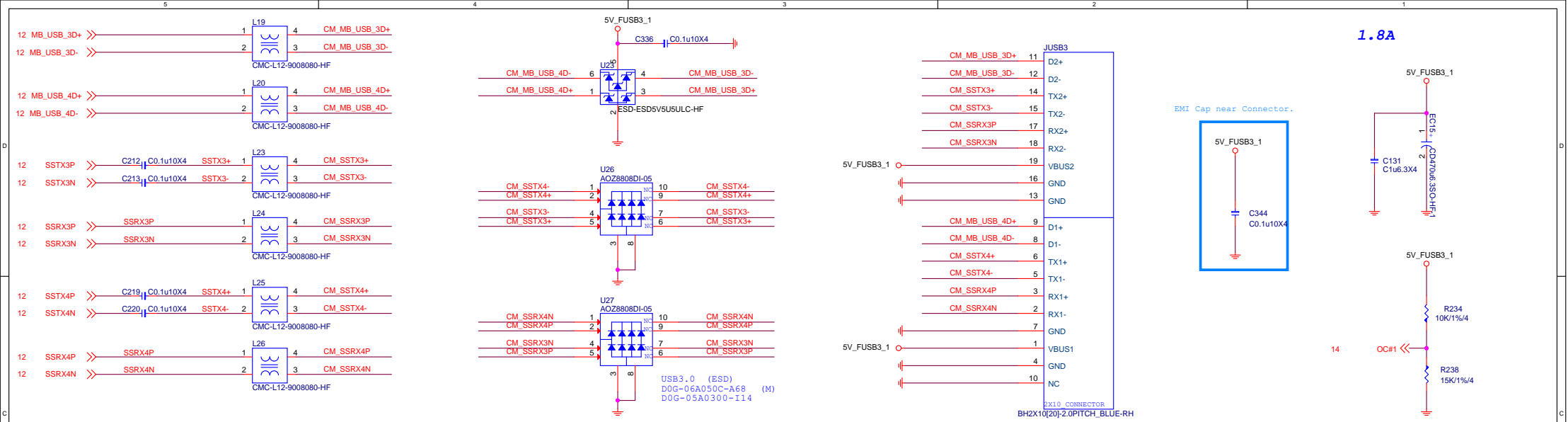
D08-2000300-P16 (Itrip=3.5A; 0.003ohm)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)



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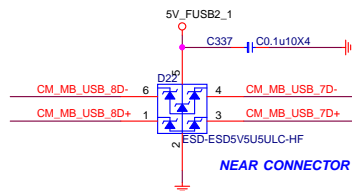
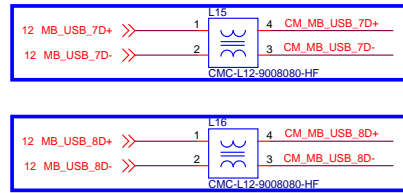
MS-7A12..

Size	Document	Description	Rev
Custom		USB POWER-MP1495/UP7501	1.1
Date:	Tuesday, November 17, 2015	Sheet 26 of 62	

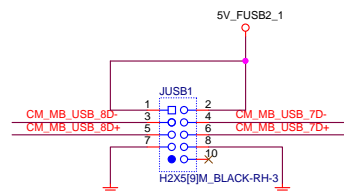
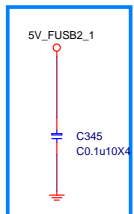


1.8A

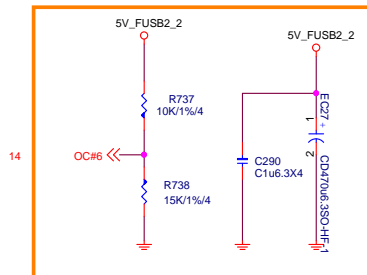
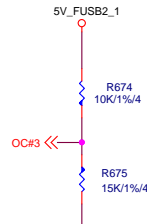
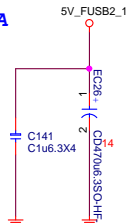
FRONT USB PORT 3,4



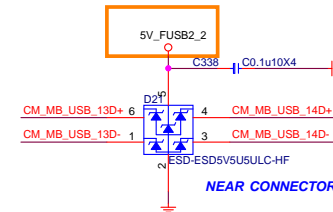
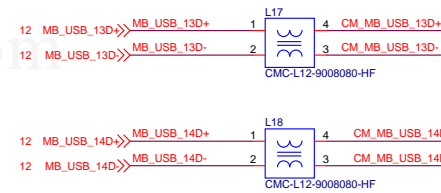
EMI Cap near Connector.



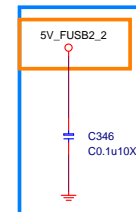
1.0A



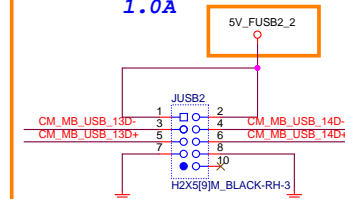
FRONT USB PORT 7,8



EMI Cap near Connector.



1.0A

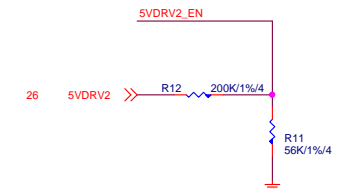


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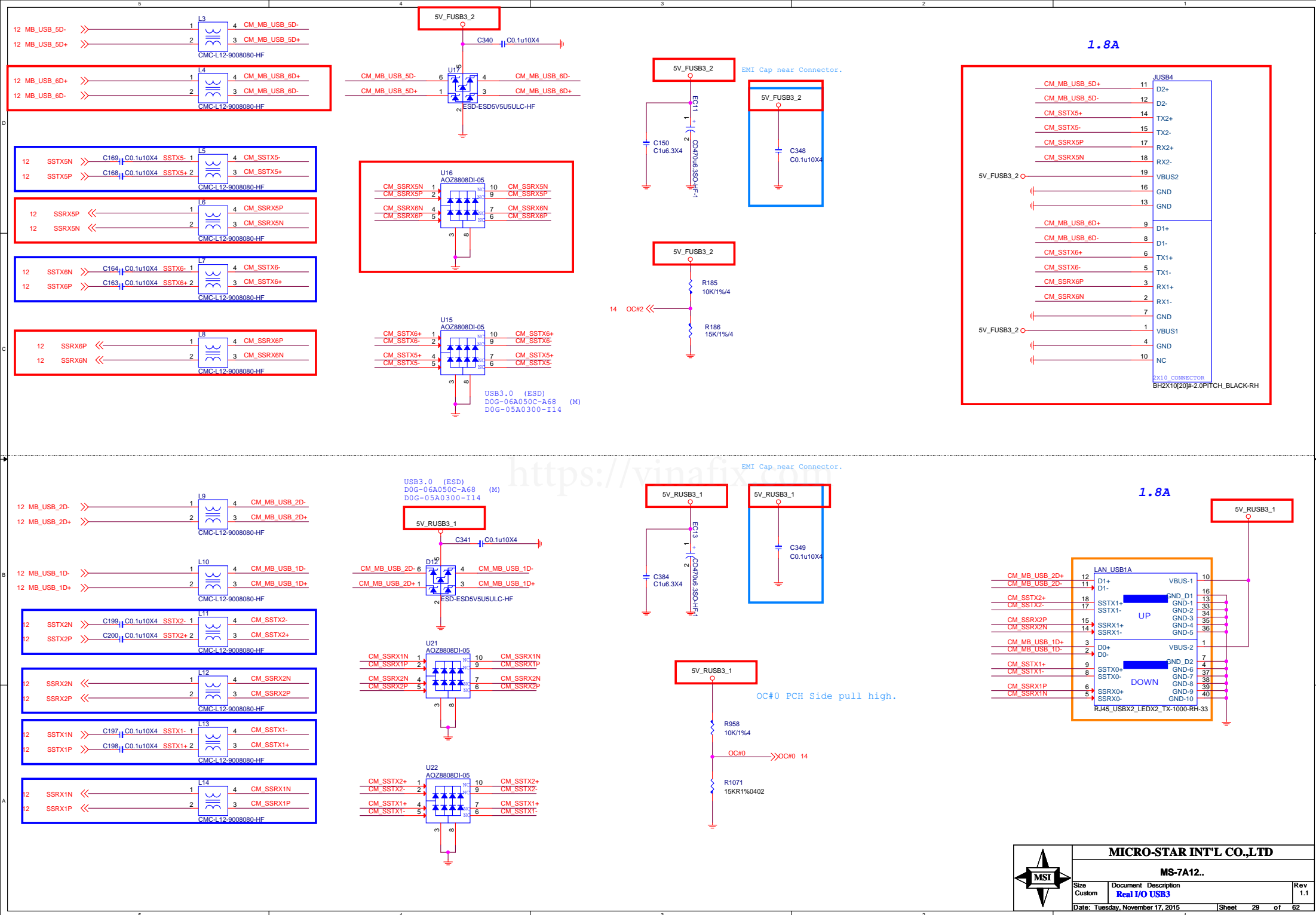
MS-7A12..

Size	Document	Description	Rev
Custom	Front	USB3/USB2	1.1
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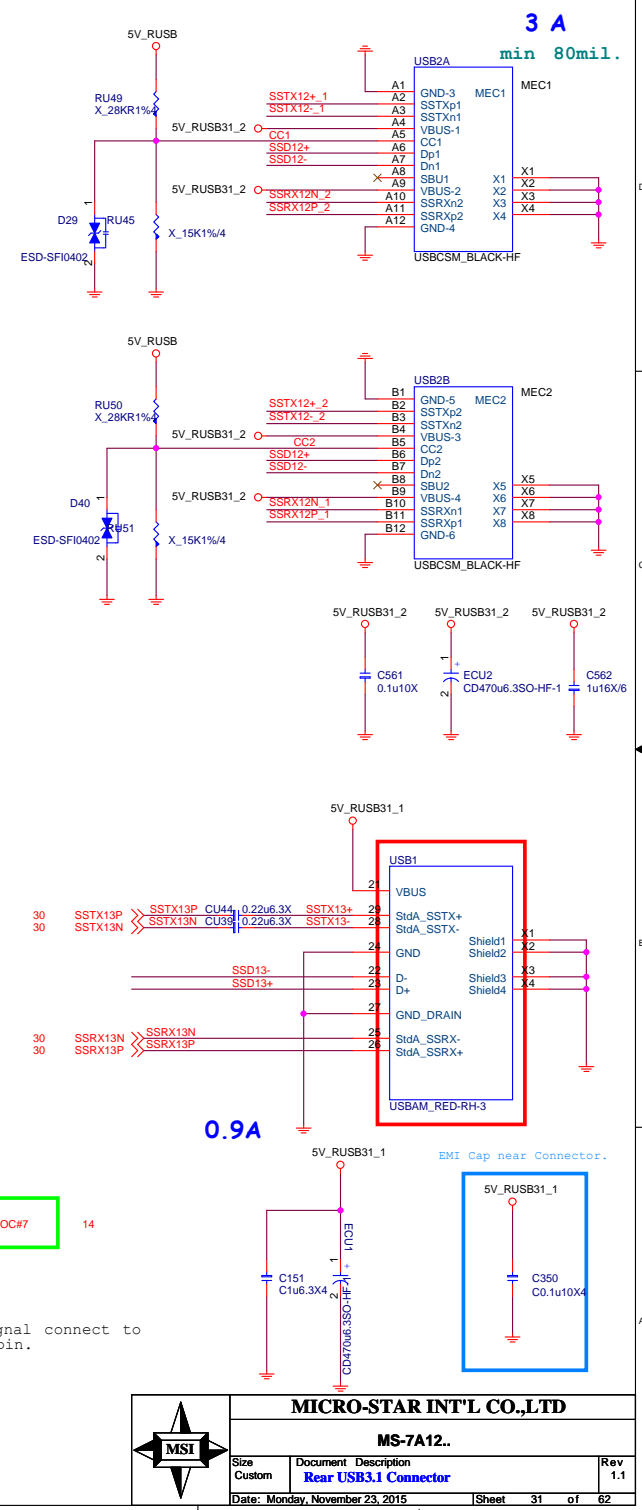
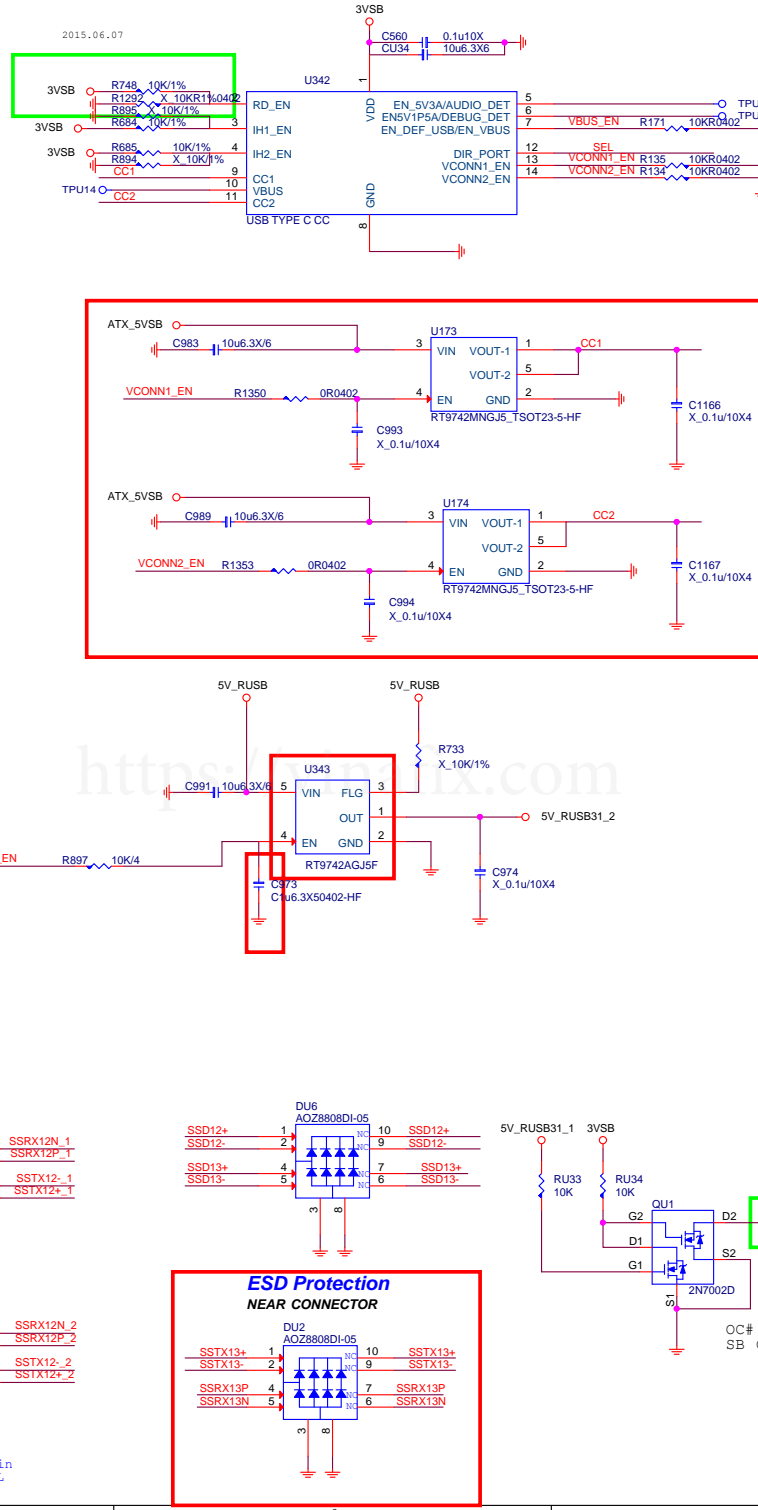
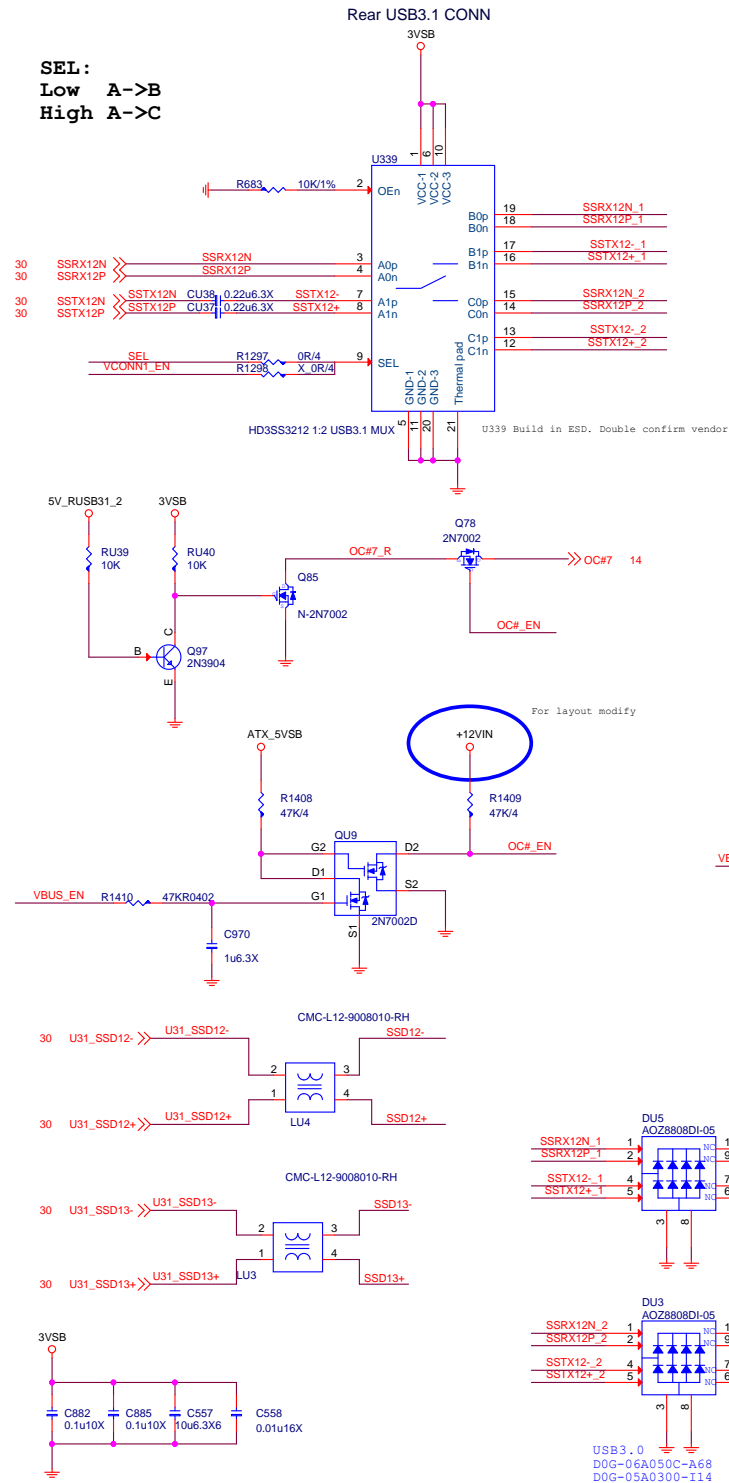
USB MODE



Size Custom	Document Description Rear I/O PS2/USB2	Rev 1.1
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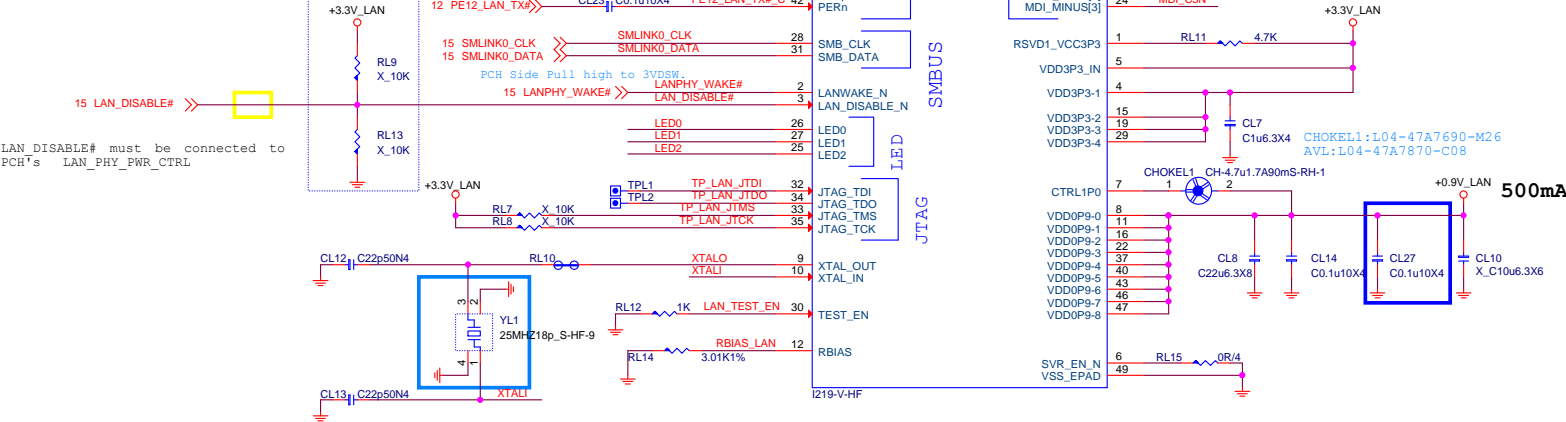

```
SEL:
Low   A->B
High  A->C
```



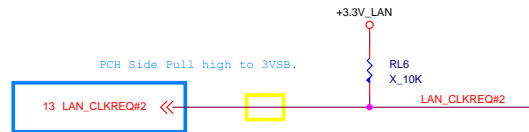
Intel I219V / I218V PHY

For EMI

Reserve RL9,RL13 for Schematic Checklists

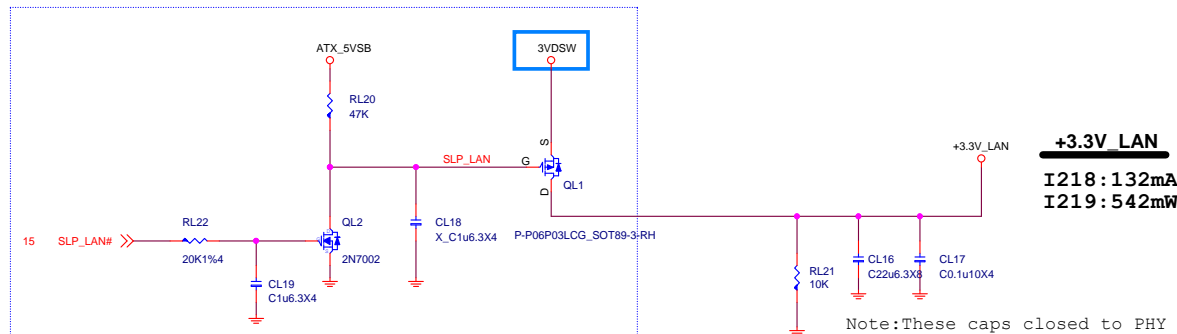


PCH's PCIECLKREQ<n> port must be mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10K to 3.3V_LAN

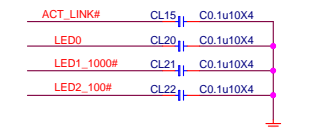


The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKREQ<n> buffer.

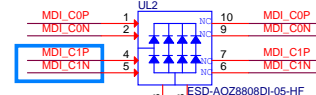
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



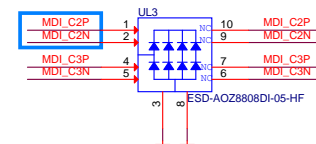
Note: These caps closed to PHY



UL2&UL3 close to connector



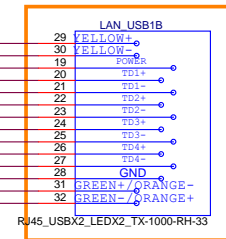
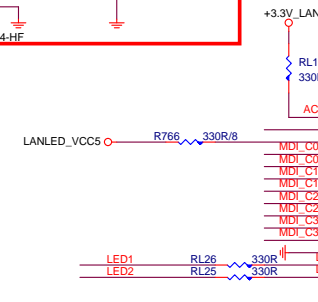
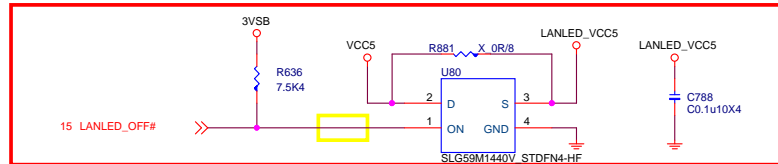
D0G-06A050C-A68
D0G-05A0300-I14



Do not pair MDI0 and MDI1 on the same TVS device (avoid LAN POE connecting issue). Other pairing combination is ok.


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Add LAN LED Cut PWR



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Custom		LAN Killer E2205	1.1
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Size	Document	Description	Rev
Custom		VGA Connector	1.1
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4	DVI_DDPCK_CLK_N	DVI_DDPCK_CLK_N	C53	C0.1U10X4	DVI_C_CLK_N	R118	470R/4	DVI_DATA_CLK
4	DVI_DDPCK_CLK_P	DVI_DDPCK_CLK_P	C54	C0.1U10X4	DVI_C_CLK_P	R120	470R/4	
4	DVI_DDPCK_TXN0	DVI_DDPCK_TXN0	C46	C0.1U10X4	DVI_C_DATA0_N	R84	470R/4	DVI_DATA0
4	DVI_DDPCK_TXP0	DVI_DDPCK_TXP0	C45	C0.1U10X4	DVI_C_DATA0_P	R97	470R/4	
4	DVI_DDPCK_TXN1	DVI_DDPCK_TXN1	C47	C0.1U10X4	DVI_C_DATA1_N	R98	470R/4	DVI_DATA1
4	DVI_DDPCK_TXP1	DVI_DDPCK_TXP1	C49	C0.1U10X4	DVI_C_DATA1_P	R111	470R/4	
4	DVI_DDPCK_TXN2	DVI_DDPCK_TXN2	C50	C0.1U10X4	DVI_C_DATA2_N	R112	470R/4	DVI_DATA2
4	DVI_DDPCK_TXP2	DVI_DDPCK_TXP2	C52	C0.1U10X4	DVI_C_DATA2_P	R117	470R/4	

U7
AOZ8808DI-05

1 10
DVI_C_DATA0_N DVI_C_DATA0_P

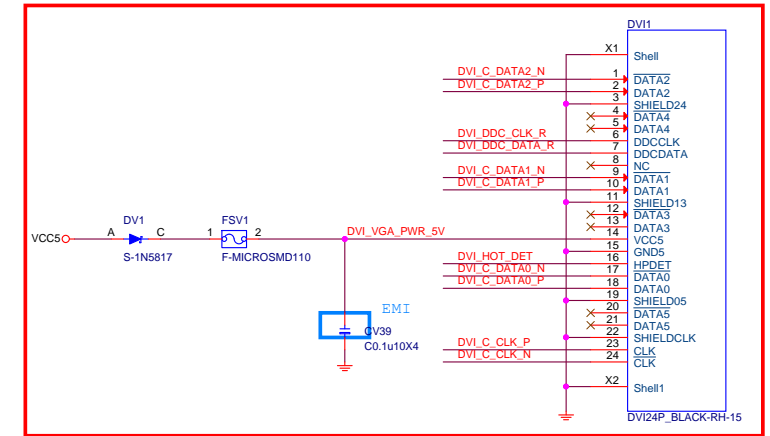
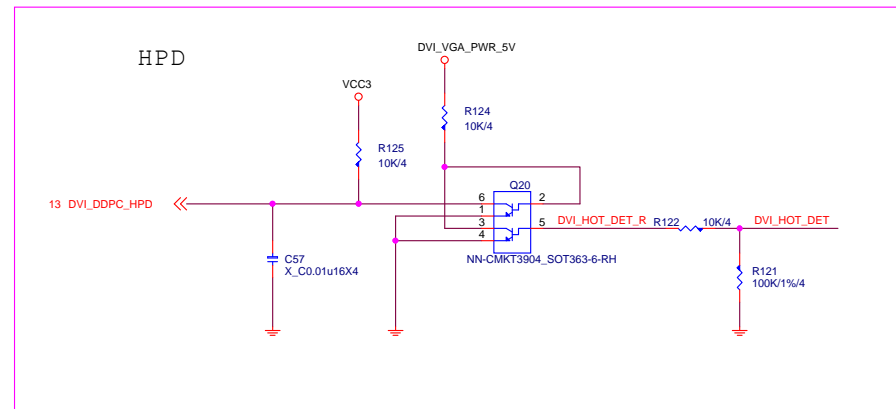
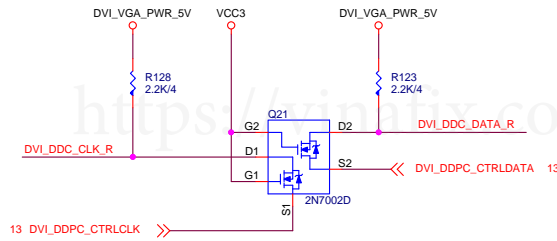
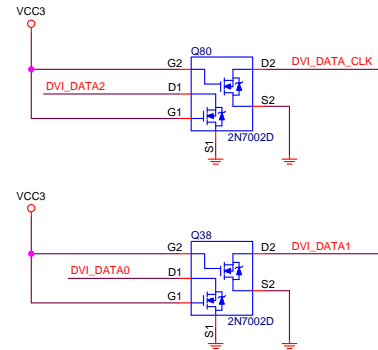
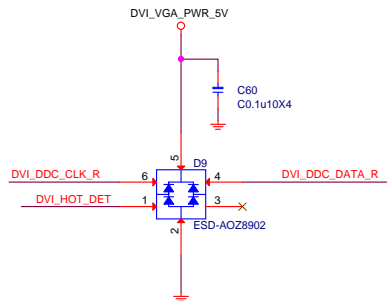
2 9
DVI_C_DATA0_P DVI_C_DATA0_P

4 7
DVI_C_DATA1_N DVI_C_DATA1_P

5 6
DVI_C_DATA1_P DVI_C_DATA1_P

3 8
NC NC

01 02



DVI_C_DATA0_N

DVI_C_DATA0_P

R96
X 243R/1%4

DVI_C_DATA1_N

DVI_C_DATA1_P

R110
X 243R/1%4

DVI_C_CLK_N

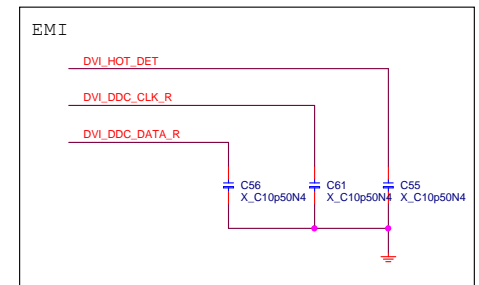
DVI_C_CLK_P

R119
X 243R/1%4

DVI_C_DATA2_N

DVI_C_DATA2_P

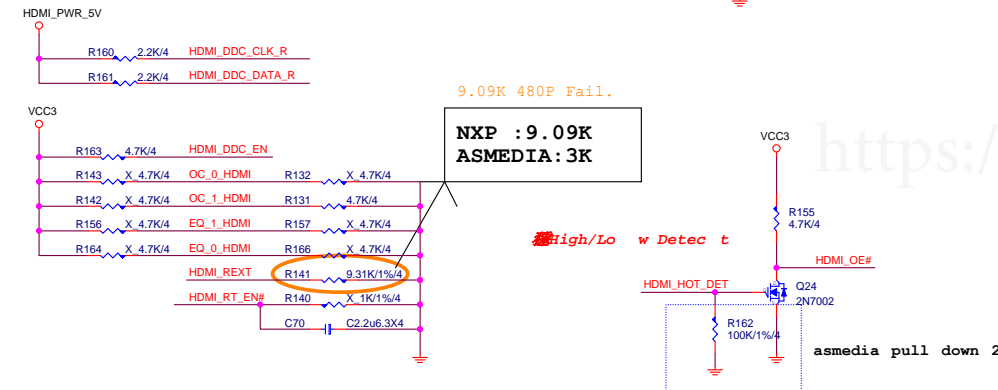
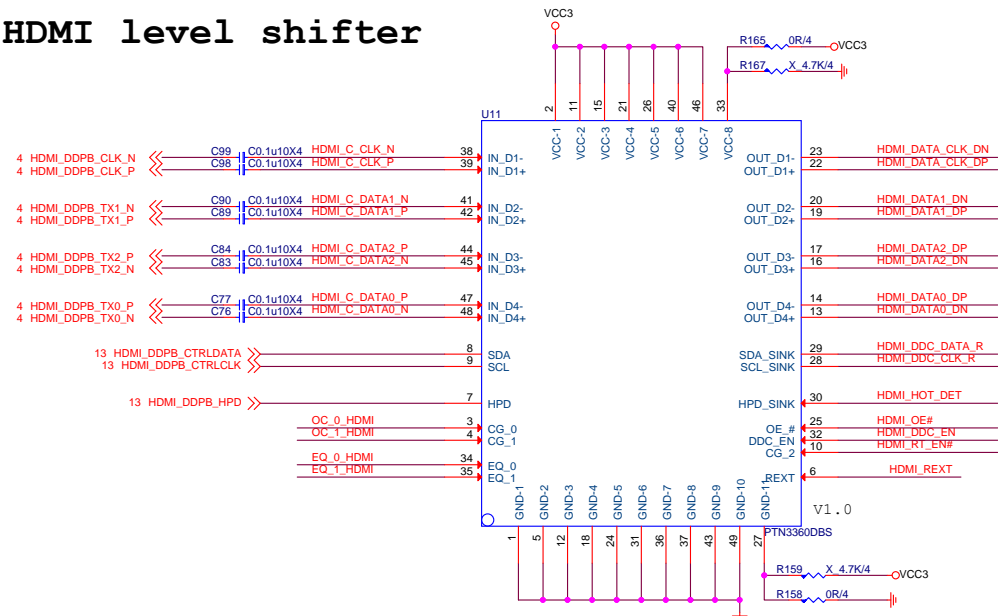
R116
X 243R/1%4



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HDMI level shifter



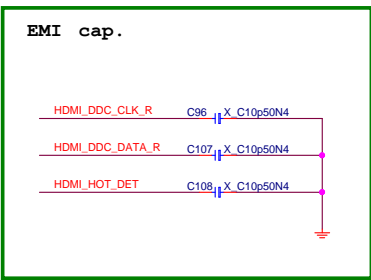
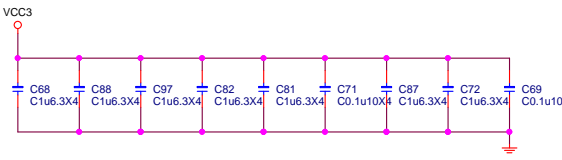
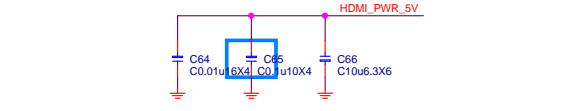
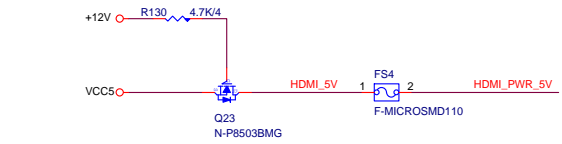
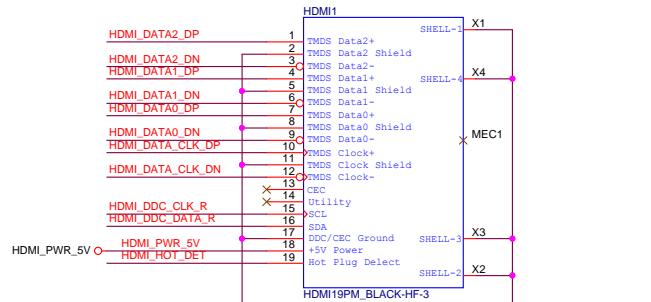
	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive	Switch	DDC Active	Buffer
1, 0, X	On		Off	
1, 1, 0	Off		On	
1, 1, 1	Off		Off	
0, X, X	Off		Off	

PC1, PC0	dB	note
00	8 dB	internal pull-up at ~500K ohm.
01	4 dB	internal pull-down at ~500K ohm.
10	12 dB	internal pull-down at ~200K ohm; 5V tolerant, internal pull-down at ~500K ohm.
11	0 dB	analog current generation.

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSPB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSPB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSPB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSPB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSPB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSPB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSPB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSPB_CLK	DDPB_3P
	DDPB_HPDI	DDSP_B_HPDI	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLCLK	HDMI_CTRL_DATA	



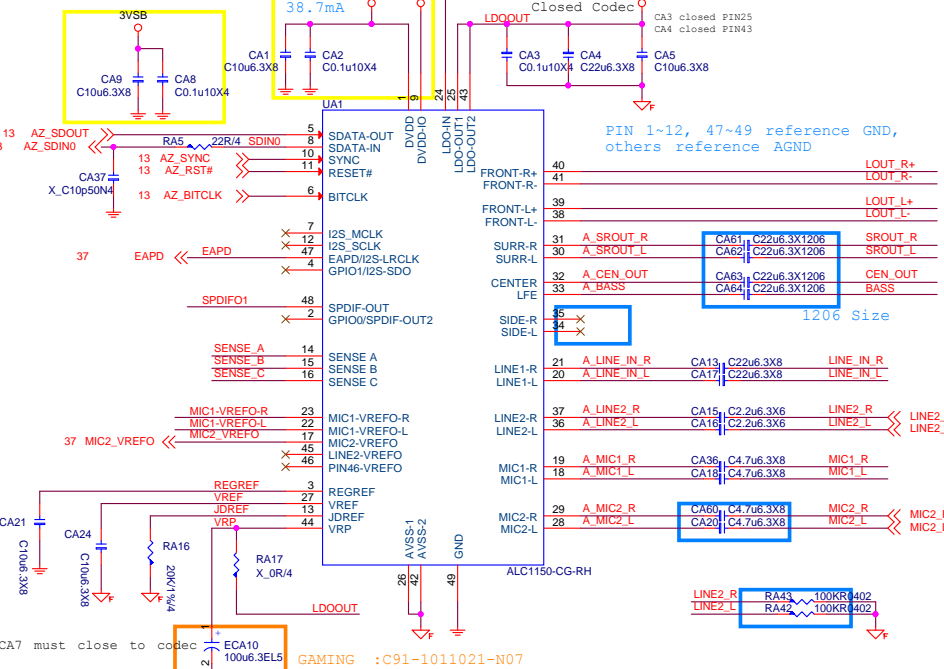
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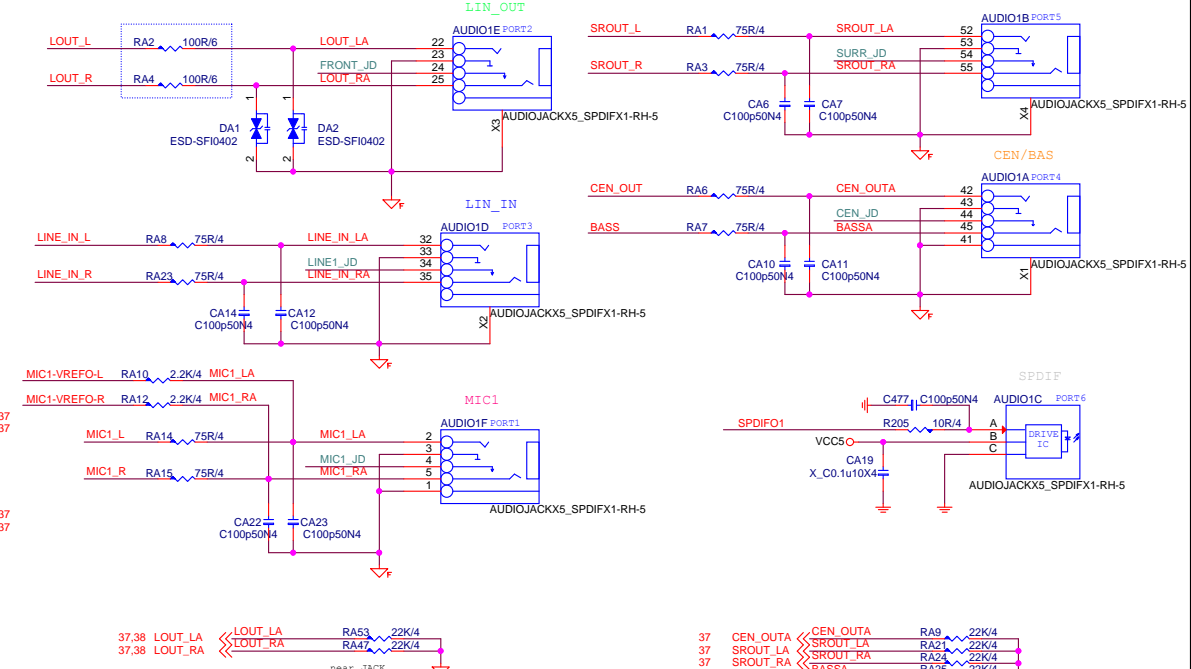
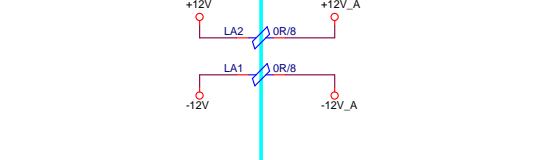
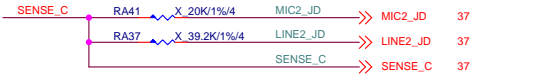
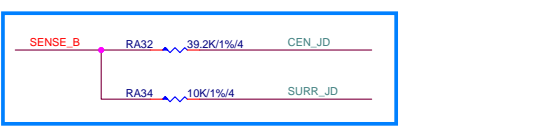
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HDMI Connector		

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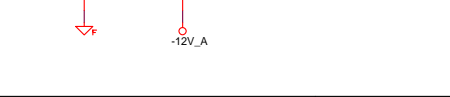
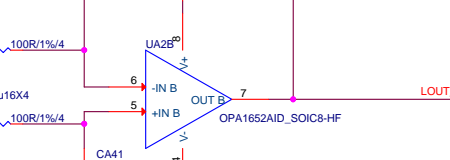
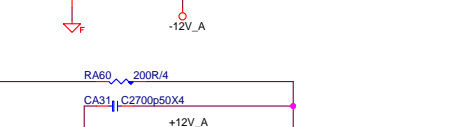
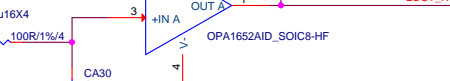
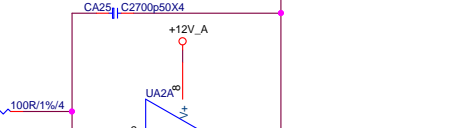
ALC1150
GAMING MODE



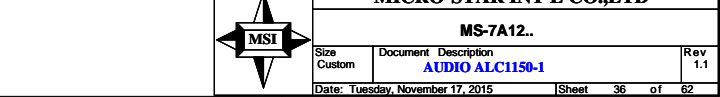
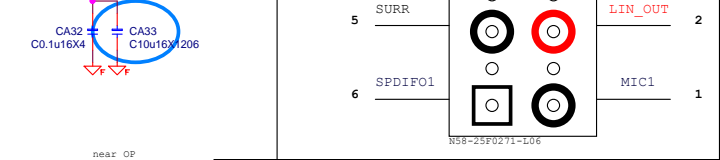
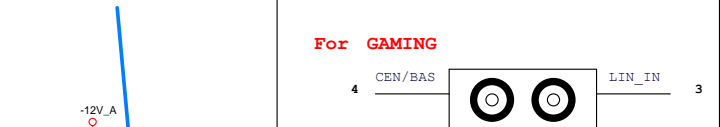
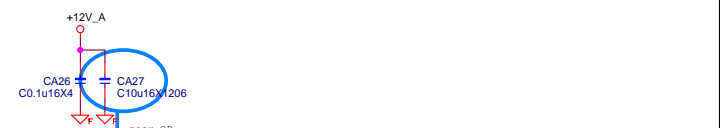
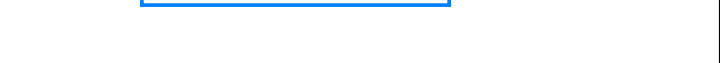
ECA7 must close to codec
GAMING :C91-1011021-N07



37,38 LOUT_LA << LOUT_LA
37,38 LOUT_RA << LOUT_RA



Remove SIDESURR.



MSI

For GAMING

4 CEN/ BAS LIN_IN 3

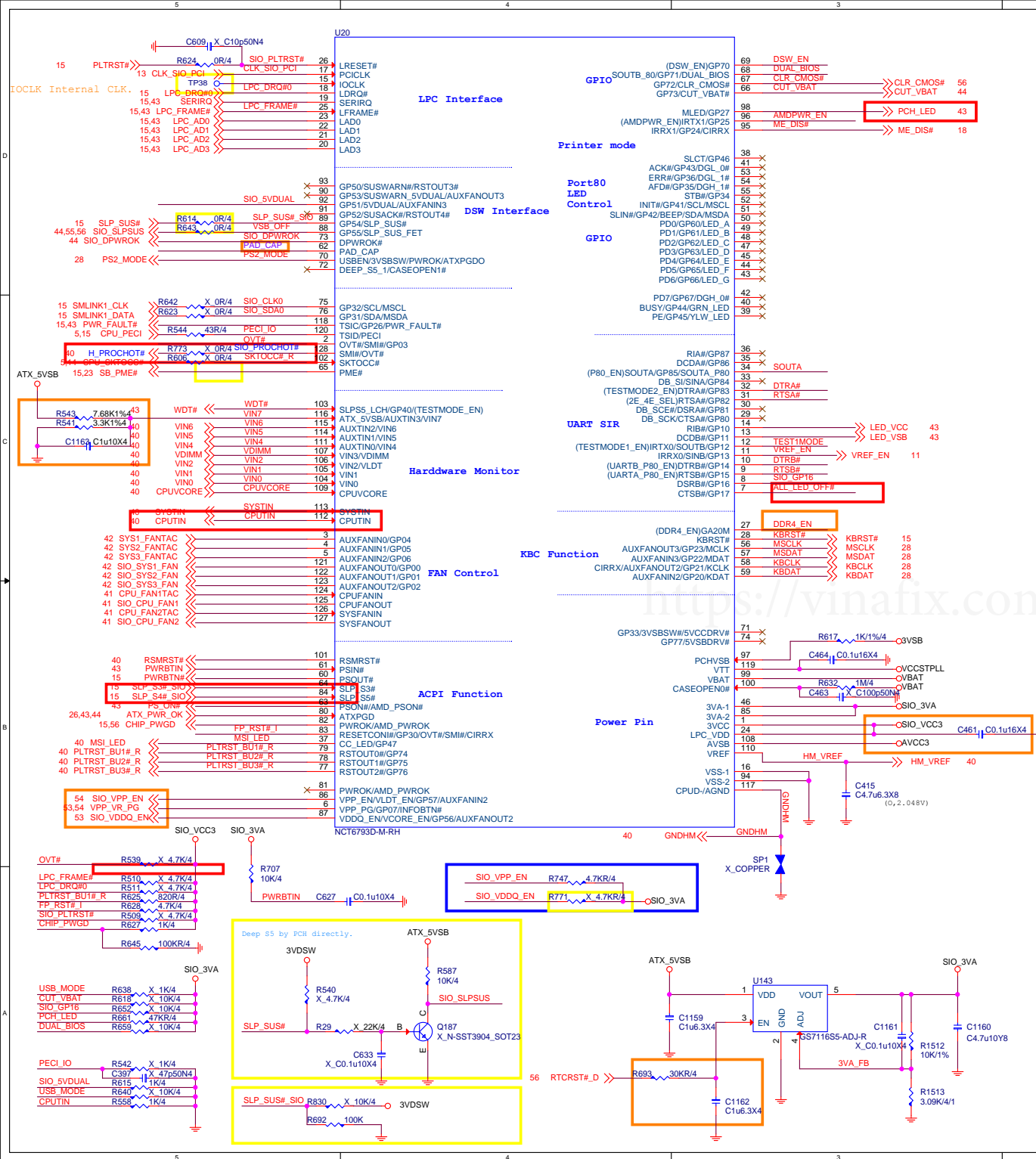
5 SURR LIN_OUT 2

6 SPDIF01 MIC1 1

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Size Custom Document Description AUDIO ALC1150-1 Rev 1.1

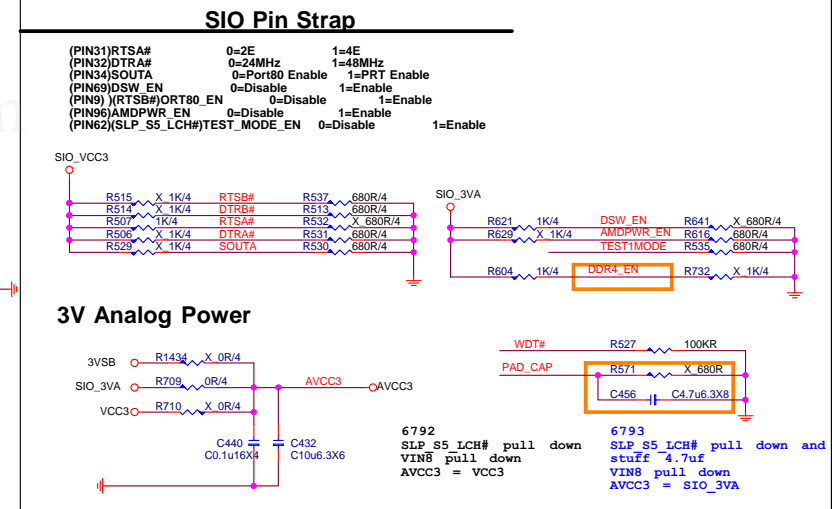
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POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMPDWR_EN	AMPDWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO



6792 SLP_S5_LCH# pull down
VIN8 pull down
AVCC3 = VCC3

6793 SLP_S5_LCH# pull down and stuff 4.7uf
VIN8 pull down
AVCC3 = SIO_3VA

Closed PIN99 Closed PIN24,108 Closed PIN46,85

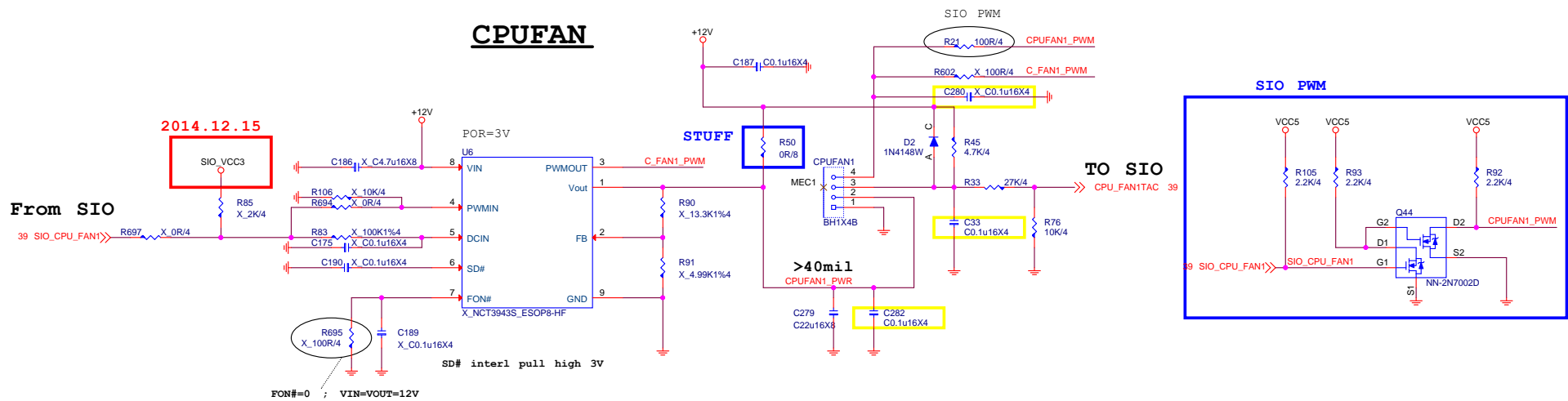
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Size	Document	Description	Rev
Custom		SIO-NTC6792D-1	1.1

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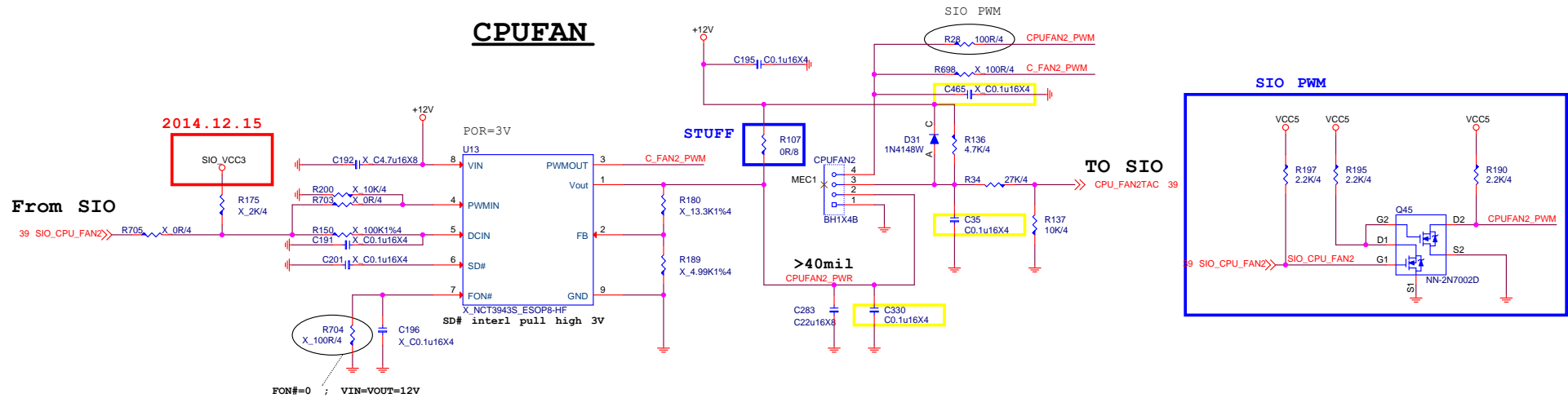
Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



WITHOUT CUT POWER

BOM OPT	R602	R21	R105	R93	R92	Q44	R697	R85	R106	R694	R83	C175	R695	C186	U6	R90	R91	R50
SIO PWM	X	o	o	o	o	o	X	X	X	X	X	X	X	X	X	X	X	o

Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)

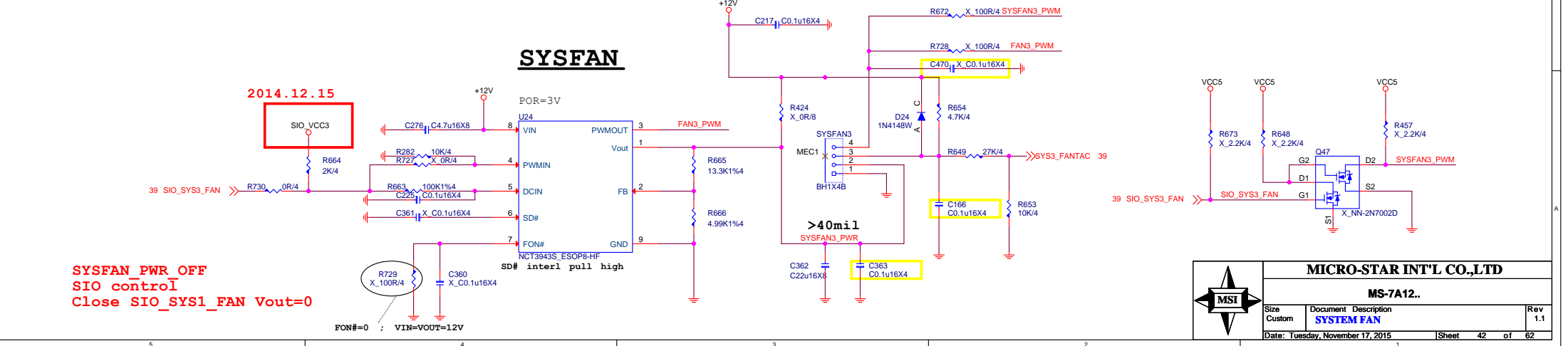
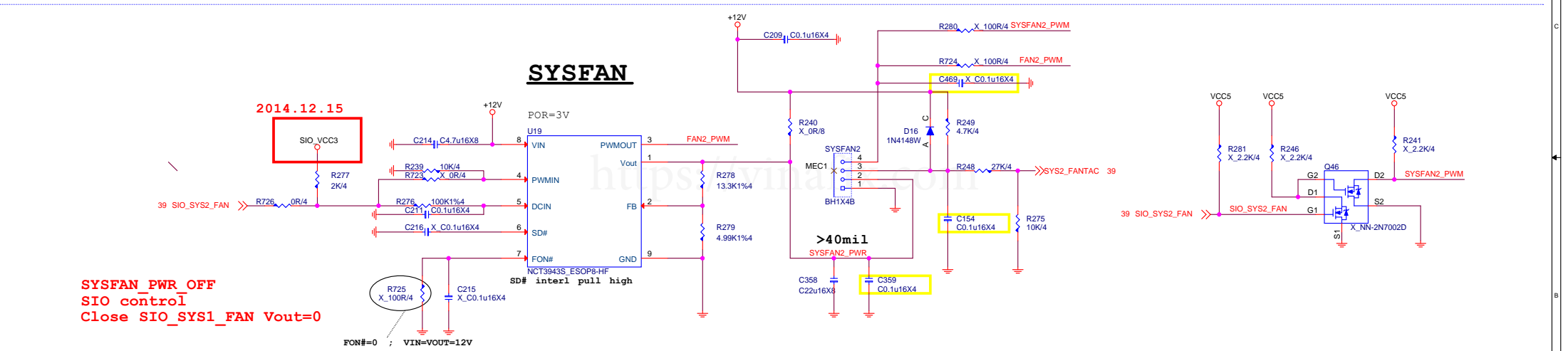
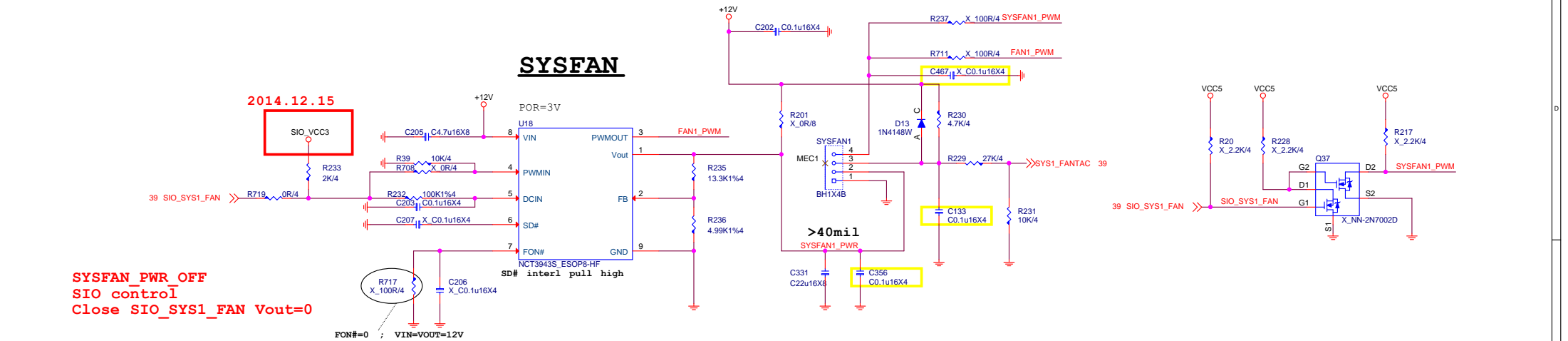


MICRO-STAR INT'L CO.,LTD

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Custom		CPU FAN	1.1
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Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

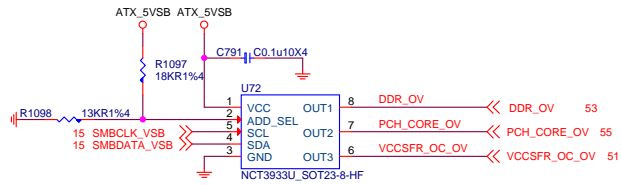


Remove Cut Power.

Vinafix.com

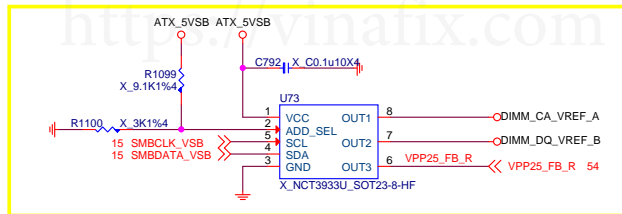
UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K



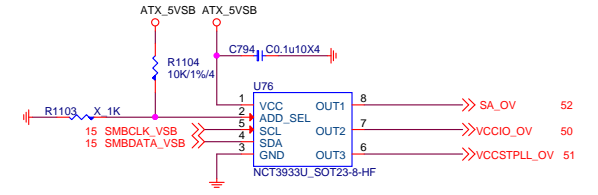
UPI VOLTAGE CONSOLE

0x28: RH=9.1K, RL=3K



UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN



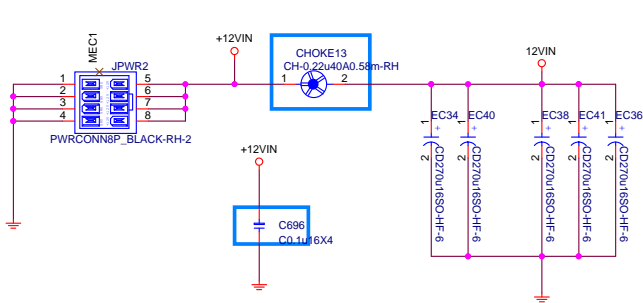
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



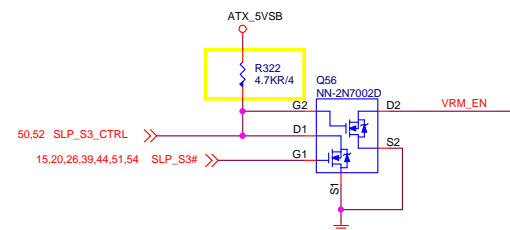
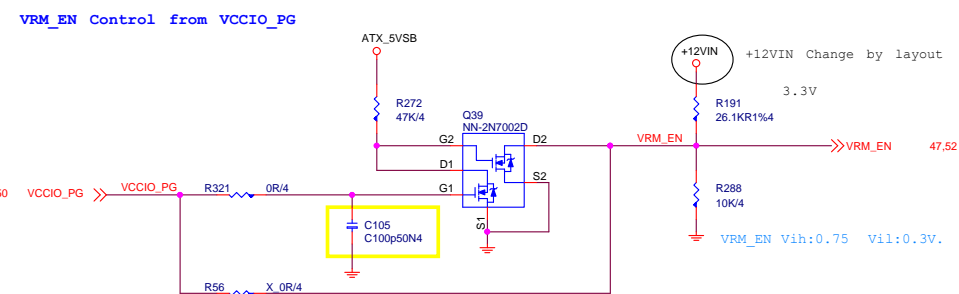
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Size	Document	Description	Rev
Custom	OV-NCT3933/GPIO-NCT5605		1.1
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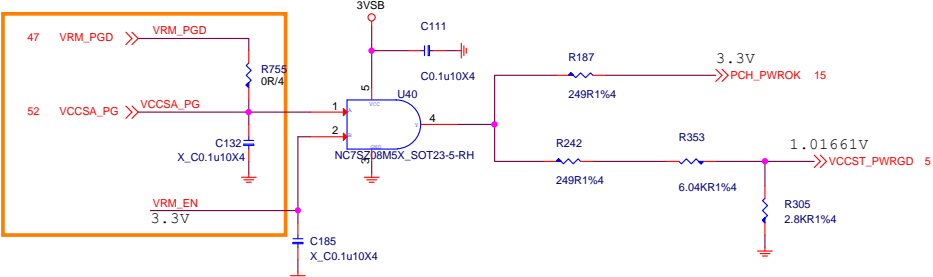


Irripble=30.95A
 VCORE 18.101A
 VGT 8.457A
 VCCSA 4.392A

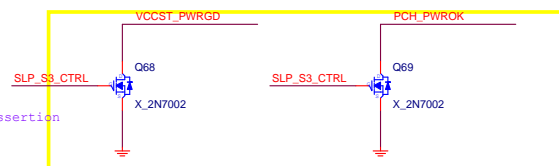


PCH_PWROK Control from VCCIO_PG&VCCSA
 VCCST_PWRGD Control from VRM_PGD

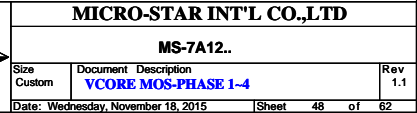
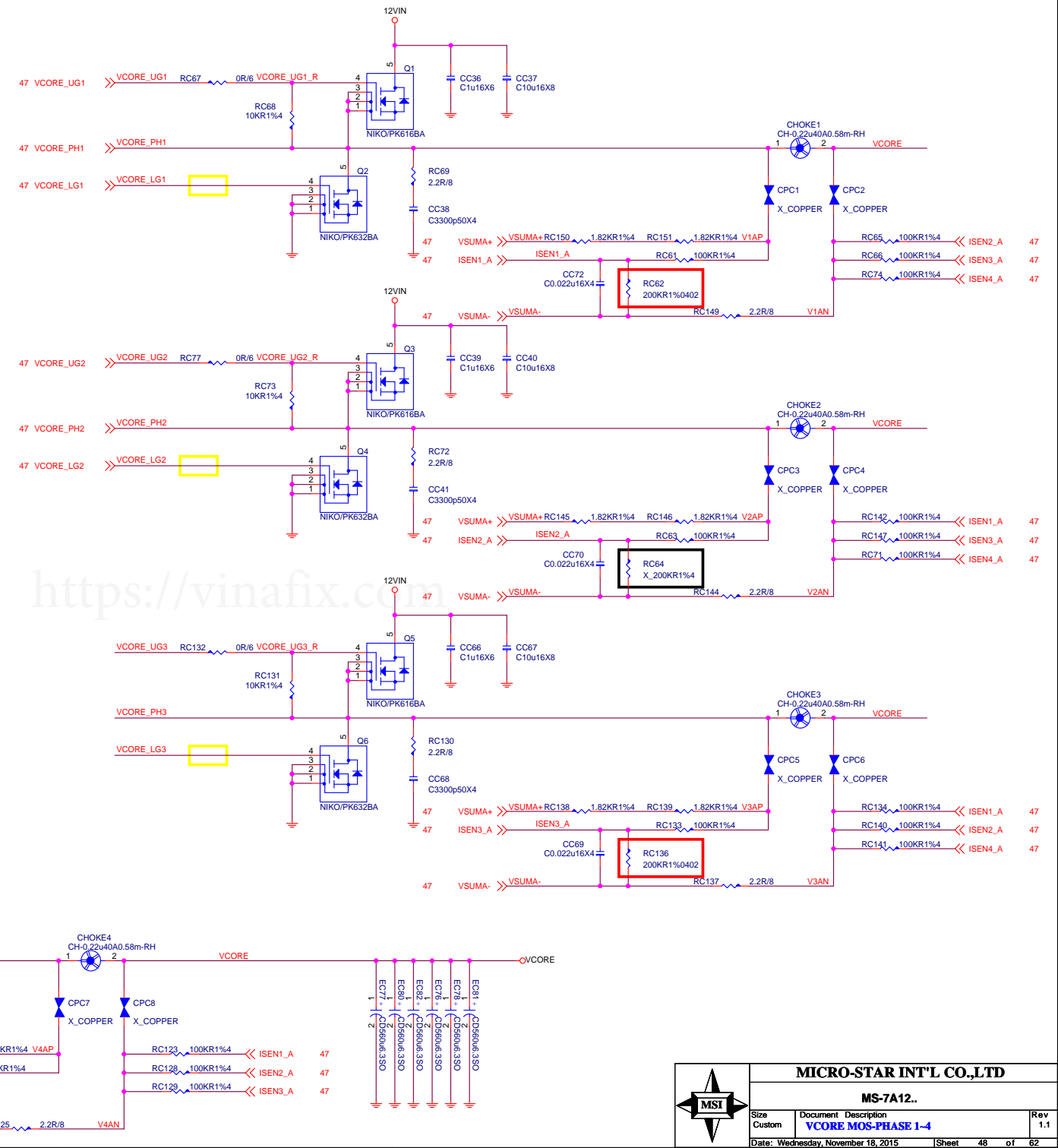
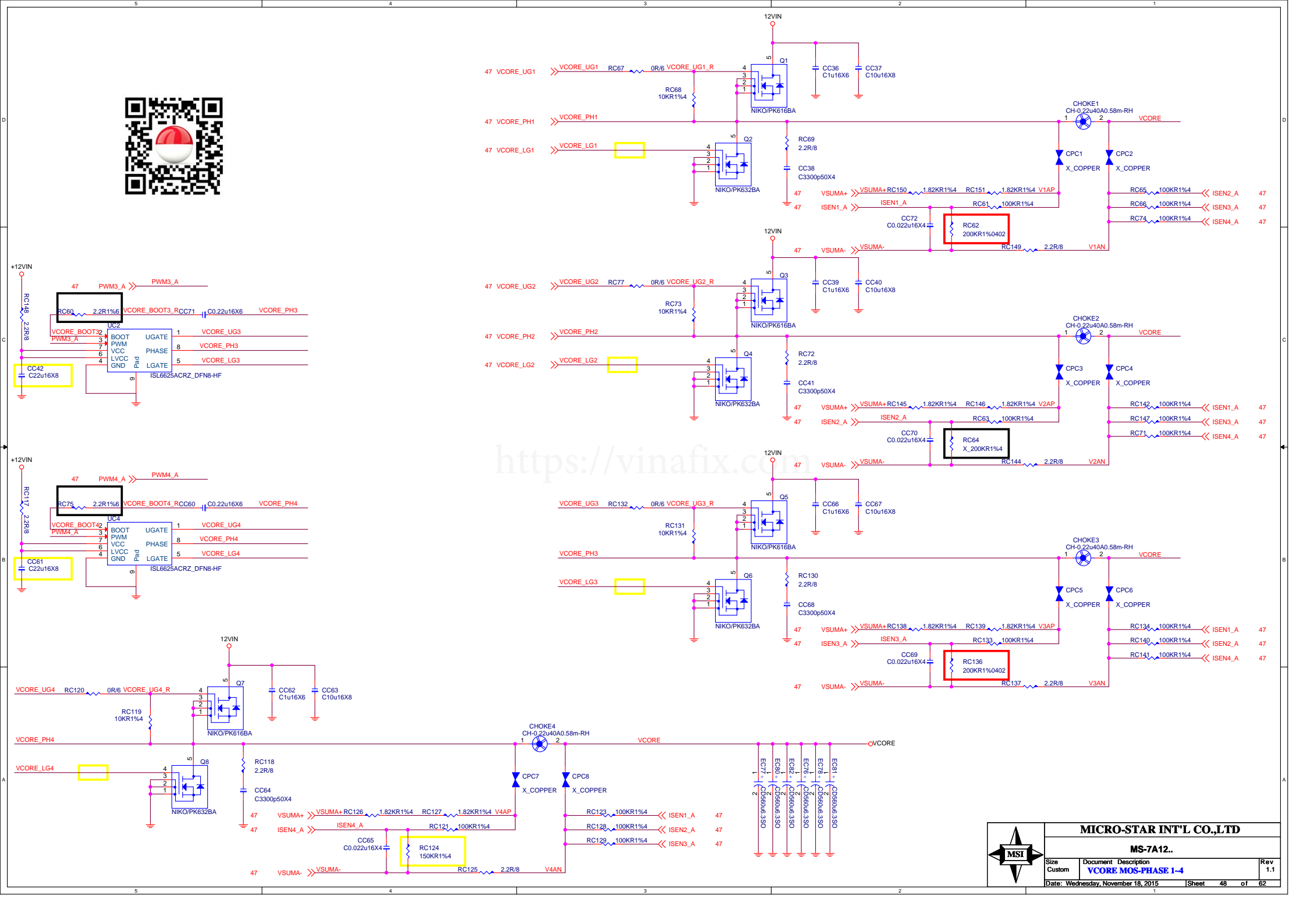
VCCSA&Vcore use same PWM IC, pull up VCC3
 VCCSA&Vcore use different PWM IC, pull up VCCSA
 VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



VCCIO 用 NB681/68 時，P IN 連接外部 VCC3
 VCCIO_PG 用一根到 0.6V，
 所以 PCH_PWROK 控制的 VCCIO_PG 改接 VRM_EN



For VCCST_PWRGD deassertion
 max:1us



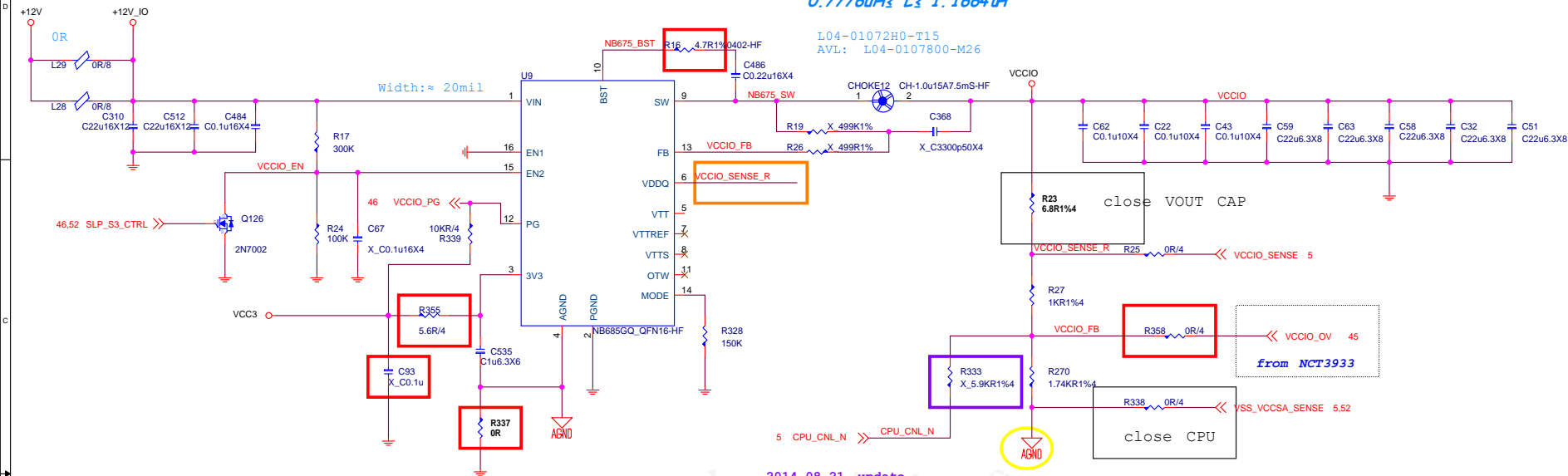
VCCIO

0.95V; 5.5A

(H110 VCCIO=VCCSA)

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

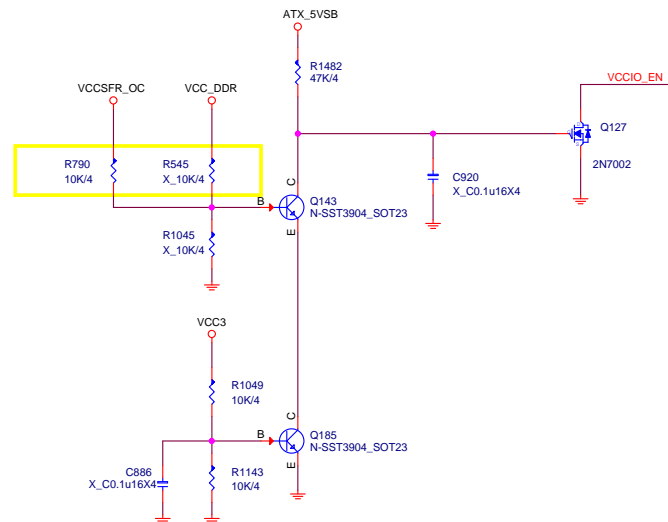
0.7776uHs Ls 1.1664uH



2014.08.21 update
RSVD for CRB
CPU_CNL_N come from CPU PROC_SELECT#

http://vinafix.com

SLP_S3# assertion to VCCIO VR disabled 4uS.
SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off. <500ms



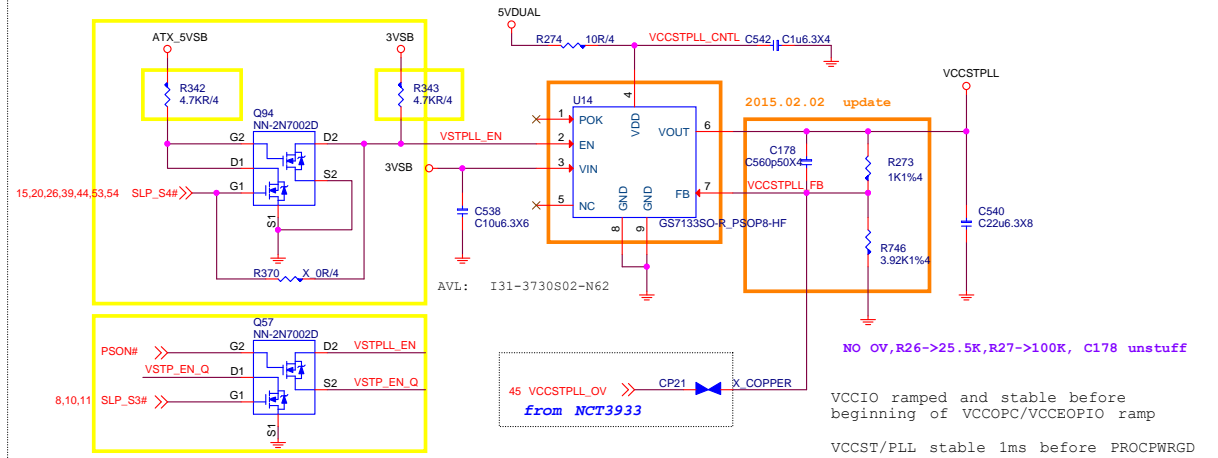
Vinafix.com

VCCSTPLL

1.0V; 250mA(0.12A+0.13A)

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO and H110

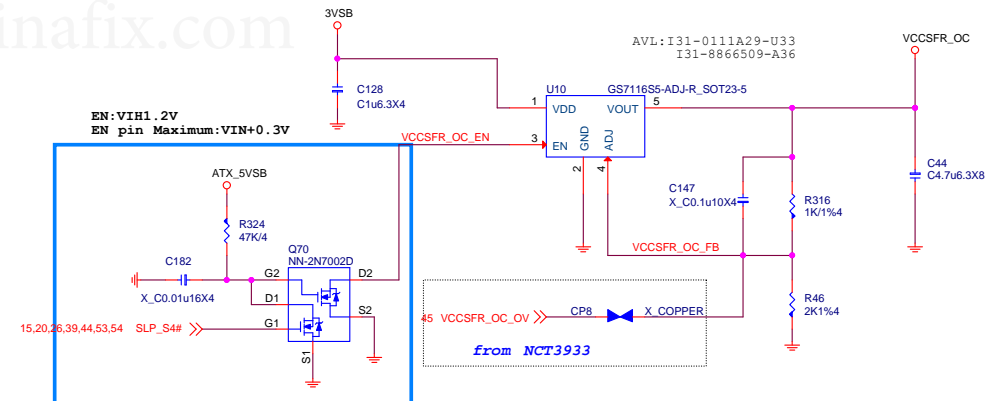


To solve CPU hotplug and lake current

VCCPLL OC

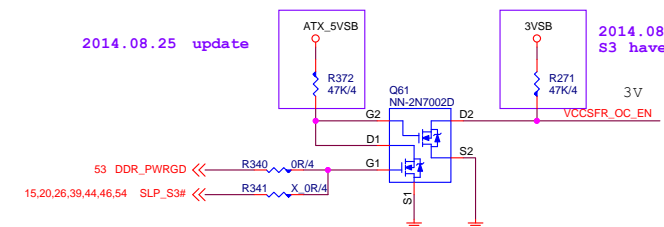
1.2V; 110mA(0.1A)

2014.08.21 update



2014.08.25 update

2014.08.25 update
S3 have power



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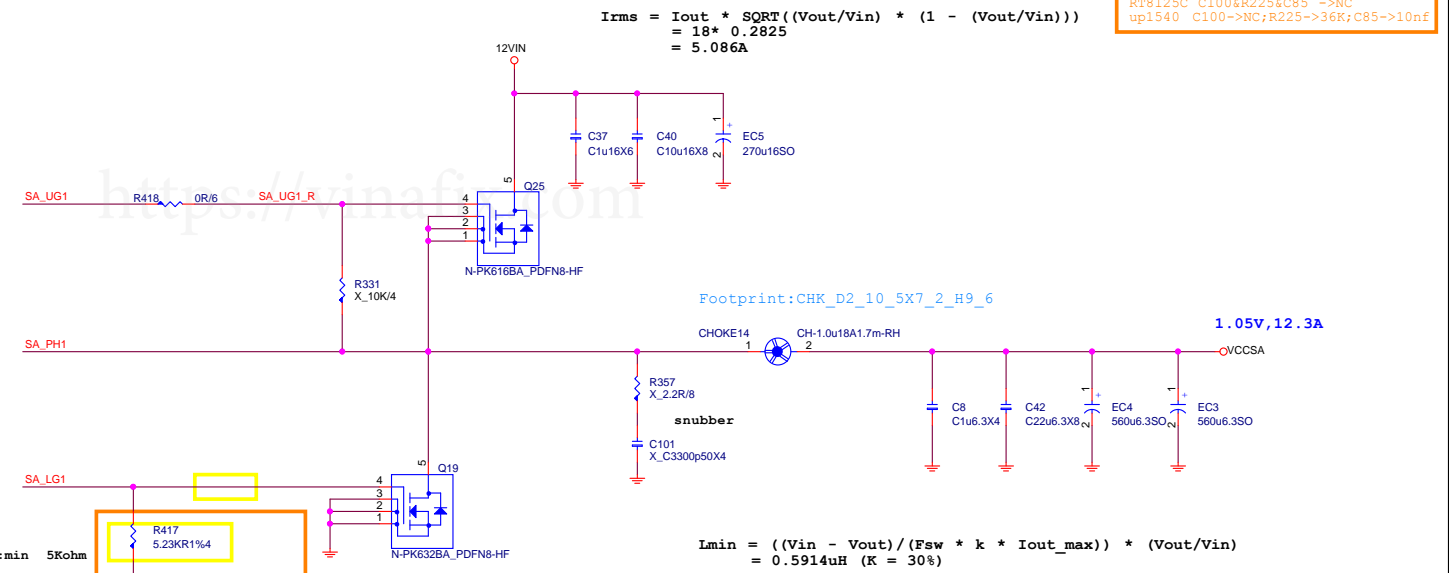
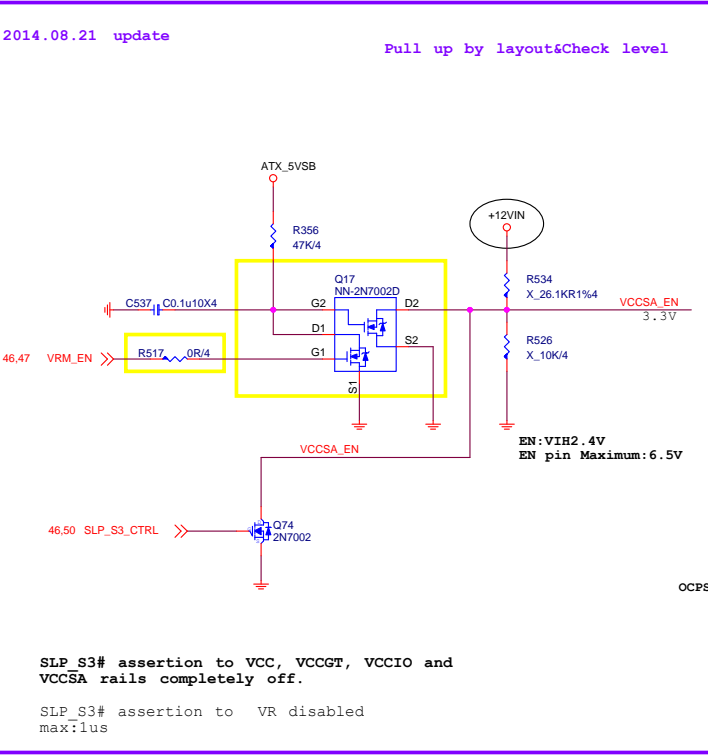
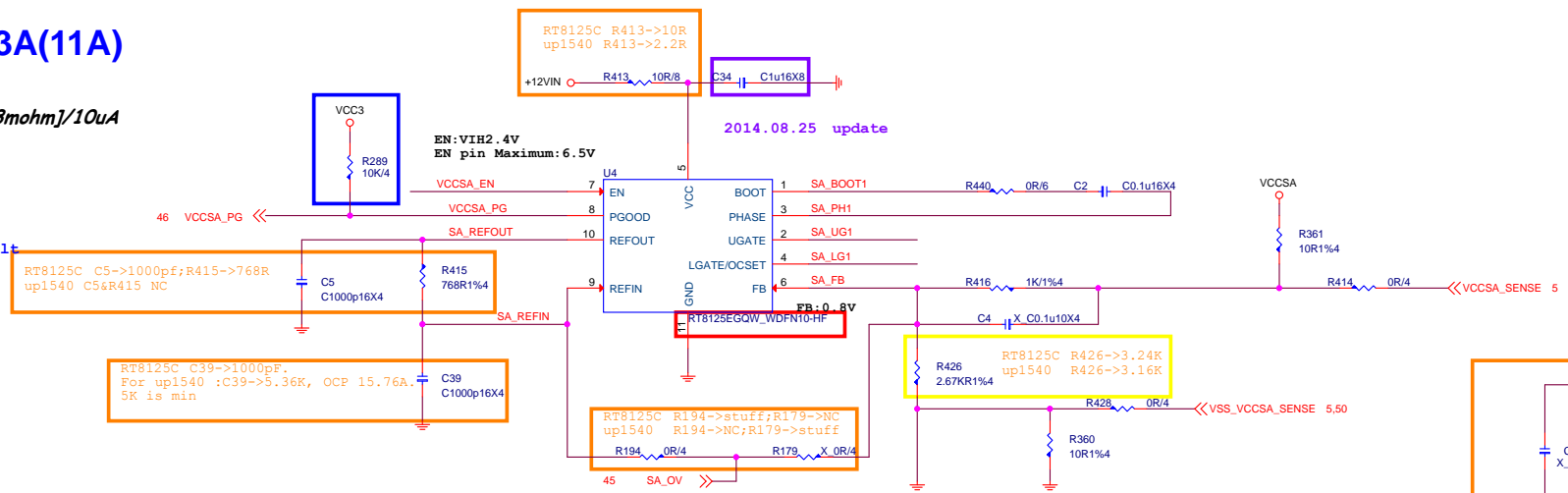
SA Power:1.05V,12.3A(11A)

$OCP = 11.1A * 1.4 = 15.54A$
 $Rocs(R15) = OCP * R_{dson}(Low\ side) 3.3m\Omega / 10\mu A$
 $= 15.54 * (3.3)m\Omega / 10\mu A$
 $= 5.1252k\Omega$

Rocs: 5.23K, OCP:
D03-4C05N03-005 : 15.38A
D03-632BA0C-N03 : 15.848A
use UBIQ MOS need Check

Rdson (low) 10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

Default

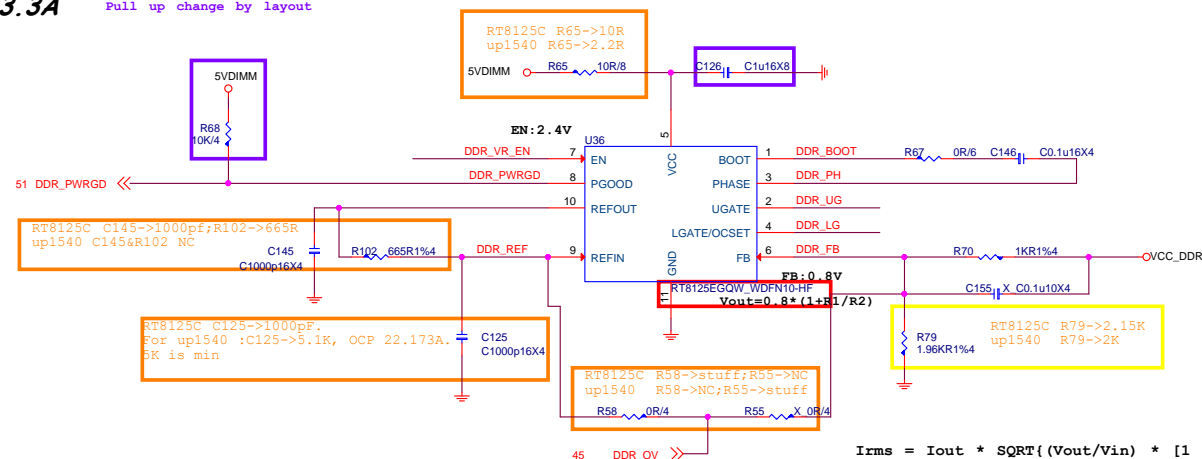


Pull up change by layout

0.1A FOR VccPLL(OC)

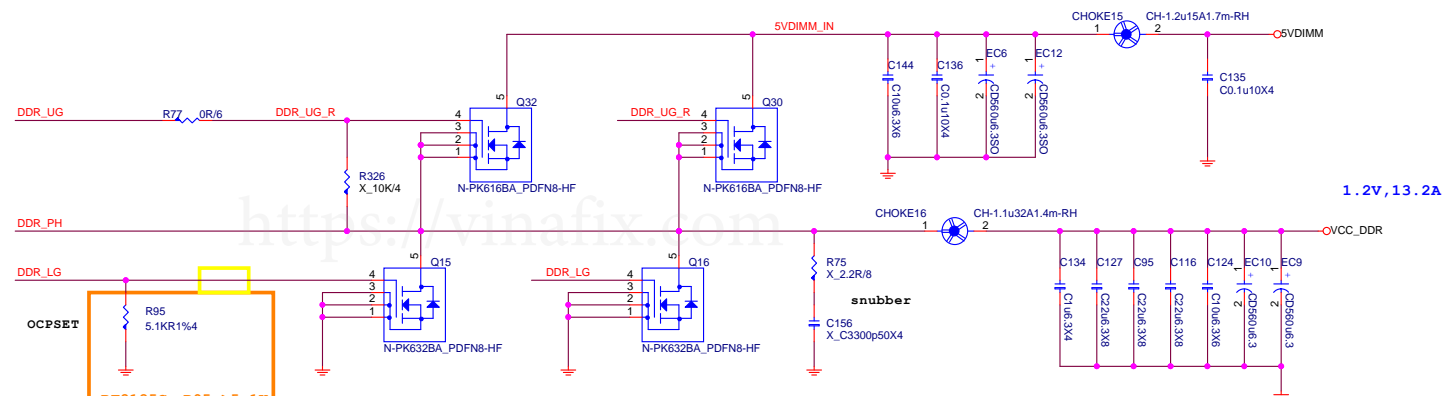
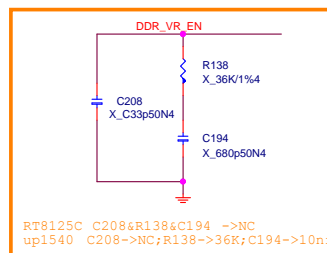
$$\begin{aligned} OCP &= 13.2A * 1.5 = 19.8A \\ R_{ocs}(R95) &= OCP * R_{ds(on)}[(Low\ side)/2]/10uA \\ &= 19.8A * (4.6/2)m\Omega / 10uA \\ &= 4.95k\Omega \approx 5K \end{aligned}$$

```
Rocpset:5.1K
OCp=Rocset*Rdson[(Low    side)/2]/10uA
=5.1K*(5/2)mohm/10uA
=22.173A
use UBIQ MOS need Check
```



```
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
      = 13.2* 0.427
      = 5.636A
```

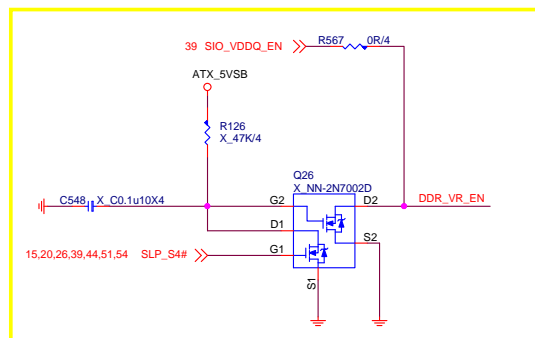
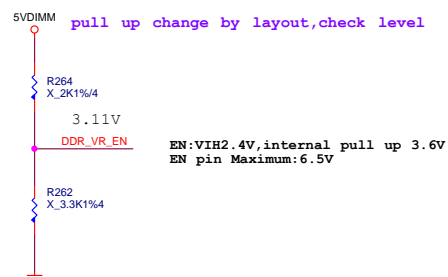
(OS-CON CAP)



Datasheet 数据表

$L_{min} = ((V_{in} - 1.2V) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$
= 0.7677uH (K = 30%)

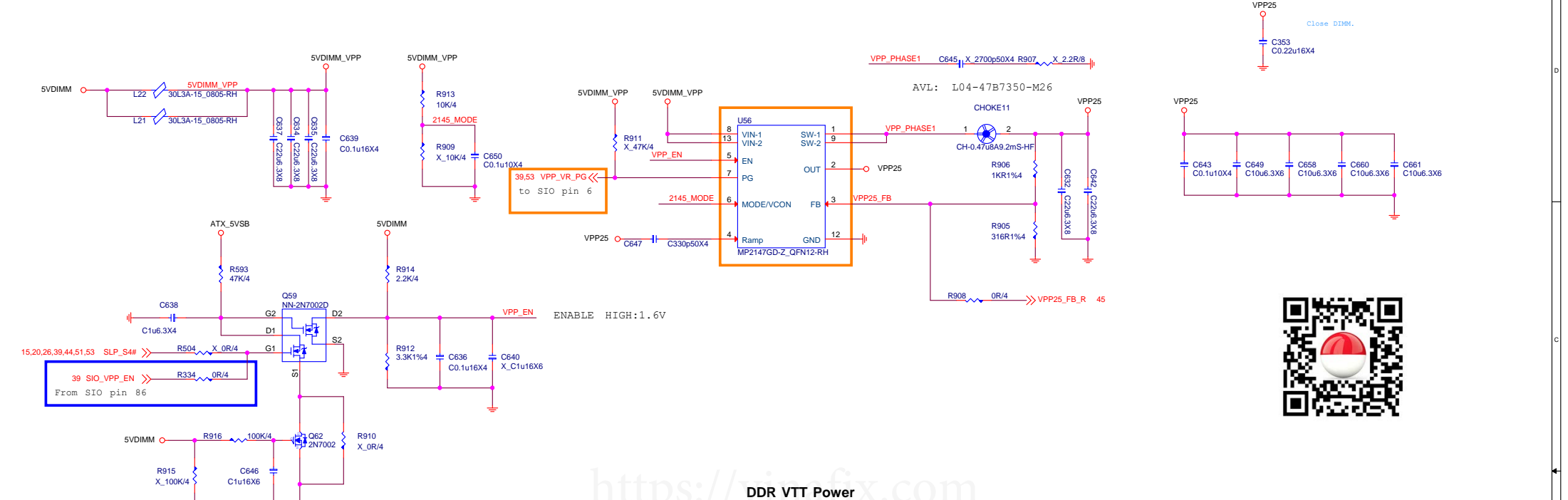
璦 C A P 璦璦璦璦, 0.242H ≤ L ≤ 1.280H



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Size Custom	Document	Description DDR POWER-RT8125C-1PHASE	Rev 1.1
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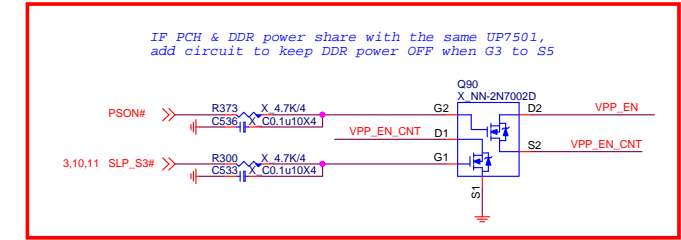
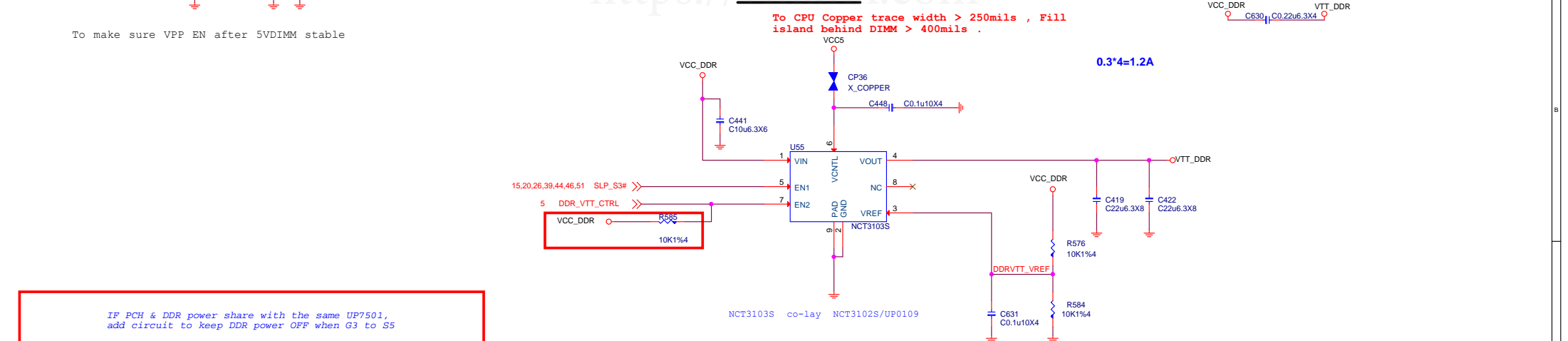
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power
2.5V; 2.24A

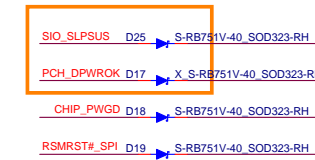


DDR VTT Power

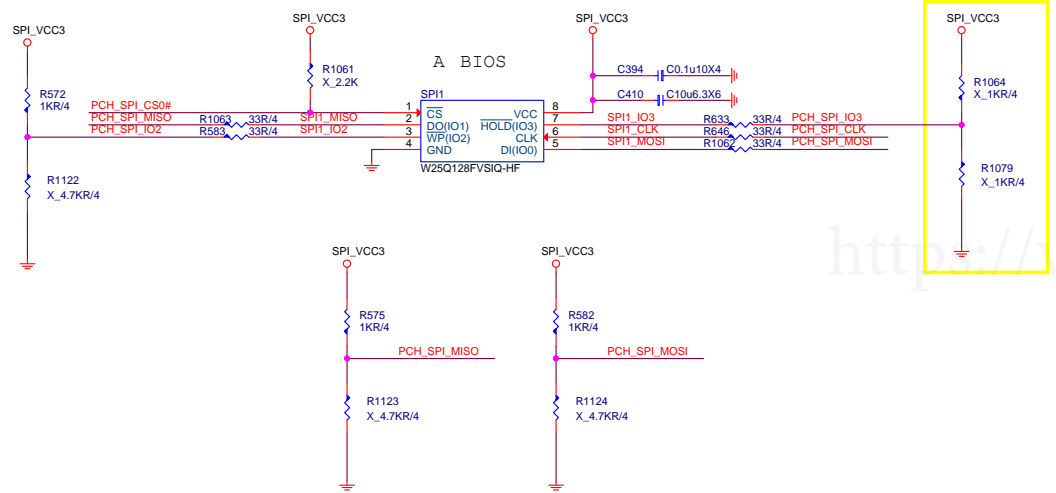
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



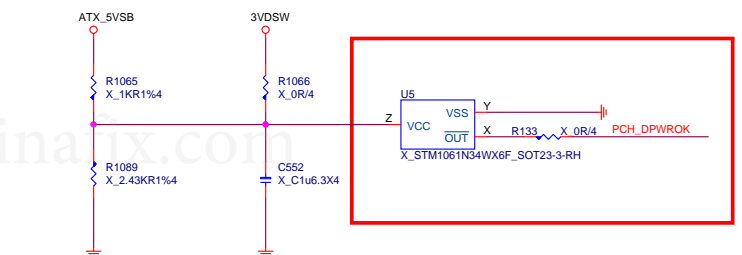
Size Custom	Document Description PCH Core Power-RT8125C	Rev 1.1
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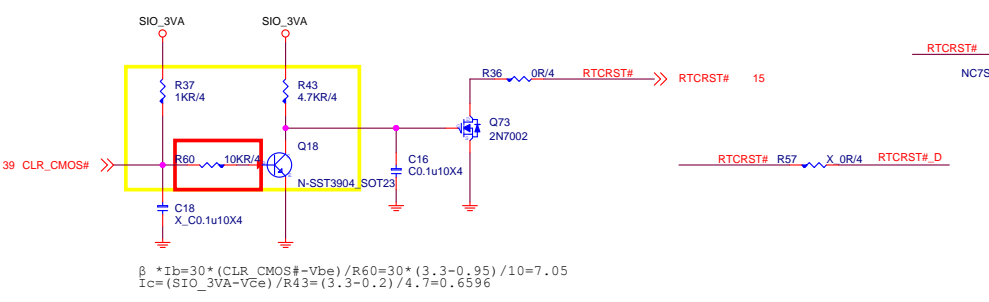
For TL624 1.1



- PCH_SPI_CS0# << PCH_SPI_CS0# 15
- PCH_SPI_CLK << PCH_SPI_CLK 15
- PCH_SPI_MISO << PCH_SPI_MISO 15
- PCH_SPI_MOSI << PCH_SPI_MOSI 15
- PCH_SPI_IO2 << PCH_SPI_IO2 15
- PCH_SPI_IO3 << PCH_SPI_IO3 15
- CHIP_PWGD << CHIP_PWGD 15,39
- PCH_DPWRCK << PCH_DPWRCK 15,44
- RSMRST#_SPI << RSMRST#_SPI 40
- SIO_SLPSUS << SIO_SLPSUS 39,44,55

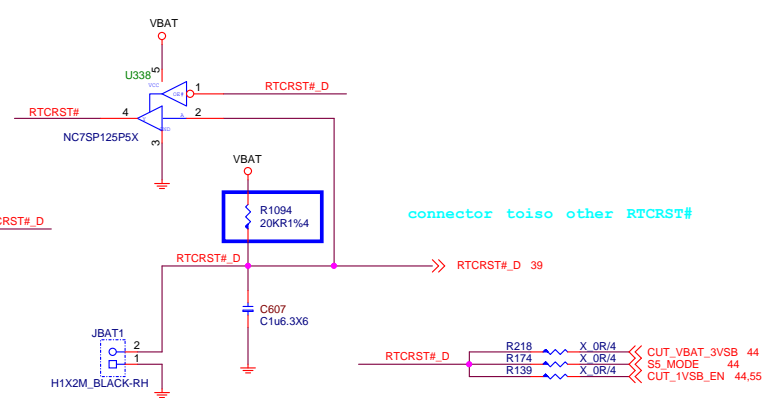


CLR_CMOS



$$\beta \cdot I_b = 30 \cdot (CLR_CMOS - V_{be}) / R_{60} = 30 \cdot (3.3 - 0.95) / 10 = 7.05$$

$$I_c = (SIO_3VA - V_{be}) / R_{43} = (3.3 - 0.2) / 4.7 = 0.6596$$



connector toiso other RTCRST#

tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R57	U338	R1094	C607
USE U338				
Auto CLR_CMOS	X	O	O	O
NOT USE U338				
Auto CLR_CMOS	O	X	X	X

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PCB P/N:PD0-07A1211-G37
PD0-07A1211-E48



CPU Socket

CPU_H1
CPU
CPU_H1

Battery

BAT1_X1
BAT-BCR2032P-RH

Audio Small Cover

COVER1
Audio Cover
E21-7978010-RH

LAN Cover

COVER2
Audio Cover
E21-7976010-RH

SLI Label

SLI_LA1
Label
X_SLI LABEL

USB3.1 Label

USB31_LA1
Label
U3.1 LABEL

Gaming Network Manager

NET_LA1
Label
Y02-MU0010170-CFO
for GAMING Pro sku+Krait sku

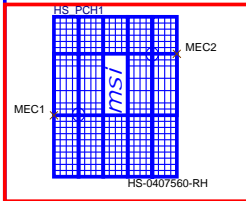
SSE

SSE_LA1
Label
Y02-MA00101-SSE

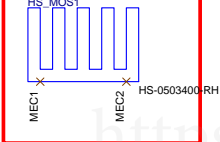
SBC Label

SBC_LA1
Label
X_SBC LABEL

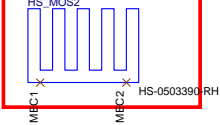
PCH Heatsink



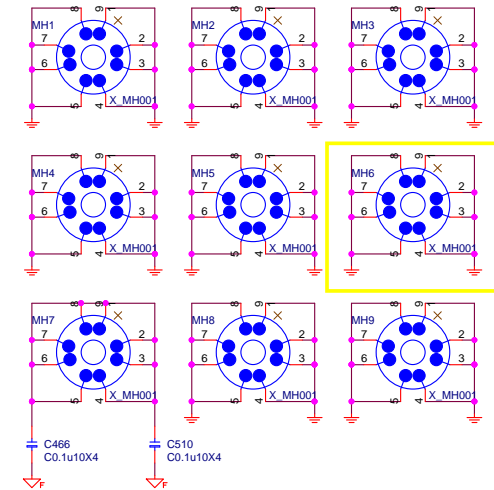
MOS1 Heatsink



MOS2 Heatsink

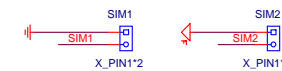


Mounting Holes



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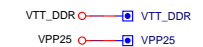
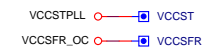
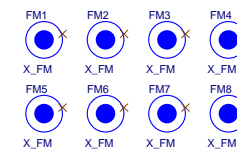
Simulation



Test point




Optical Fiducial Marks-120



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Custom	Manual parts		1.1
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<https://vinafix.com>

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			MS-7A12..		
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Custom		XDP&EMI CAP			1.1
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